MLX90293 Linear Hall Position Sensor IC

Datasheet

Features and Benefits

- Linear Hall Position Sensor IC
- Non-linear Magnetic Design with Linear Output Signal
- Programmable Transfer Characteristic to compensate system non-linearity and thermal drift:
  - Over Position : 16 segments – Piece-Wise-Linear
  - Thermal Drift over Temperature : Sensitivity and Offset : 6 segments - Piece-Wise-Linear[(1)]
- Selectable Output Mode:
  - Analog (Ratiometric)
  - Pulse Width Modulation (PWM)
  - SENT (according to SAE J2716-2010)
- 12 bit Resolution - 10 bit Thermal Accuracy
- Open/Short Diagnostics
- Over-Voltage Protection
- Under-Voltage Detection
- 48 bit ID Number option
- AEC-Q100 Qualified
- Single Die – SOIC-8 Package RoHS Compliant
- Dual Die (Full Redundant) – TSSOP-16 Package RoHS Compliant

SOIC-8

TSSOP-16

Applications

- Absolute Small Angle Rotary Position Sensor
- Absolute Small Stroke Linear Position Sensor
- Pedal Position Sensor
- Non-Contacting Potentiometer

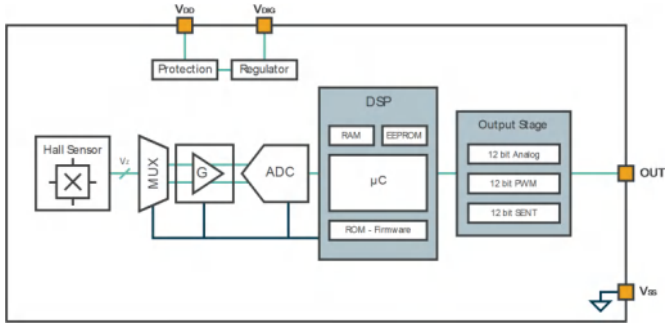
Description

The MLX90293 is a SMD Programmable Linear Hall Sensor IC that enables contact less position sensor applications.

The sensor measures the magnetic field component perpendicular to the surface of the IC. The MLX90293 supports multiple output modes, such as analog, PWM and SENT 2010.

The MLX090293 enables extensive nonlinear optimization of the transfer characteristic. Such optimization in turn enables simplified magnetic designs. The result is a linear output characteristic over position after calibration.

The customer can program this relation in his end-of-line calibration through the connector with Melexis tooling.



1 IC is trimmed at Melexis to achieve minimized IC sensitivity & offset drift over temperature. Customers can trim the sensitivity & offset drift of the application over temperature.

Melexis
INSPIRED ENGINEERING

Contents

1. Ordering Information

Product Code	Temperature Code	Package Code	Option Code	Packing Form
MLX90293	E	DC	ADM-000	RE
MLX90293	L	DC	ADM-000	RE
MLX90293	E	GO	ADM-000	RE
MLX90293	L	GO	ADM-000	RE
MLX90293	E	DC	ADM-100	RE
MLX90293	L	DC	ADM-100	RE
MLX90293	E	GO	ADM-100	RE
MLX90293	L	GO	ADM-100	RE

Legend:

Temperature Code:	E: from -40 Deg.C to 85 Deg.C L: from -40 Deg.C to 150 Deg.C
Package Code:	"DC" for SOIC-8 package "GO" for TSSOP-16 package (dual die)
Option Code:	ADM-000 – Default ADM-100 – Low thermal drift
Packing Form:	"RE" for Reel "SP" for Sample Pack
Ordering Example:	MLX90293LGO-ADM-100-RE

Table 1 - Legend

2. Functional Diagram

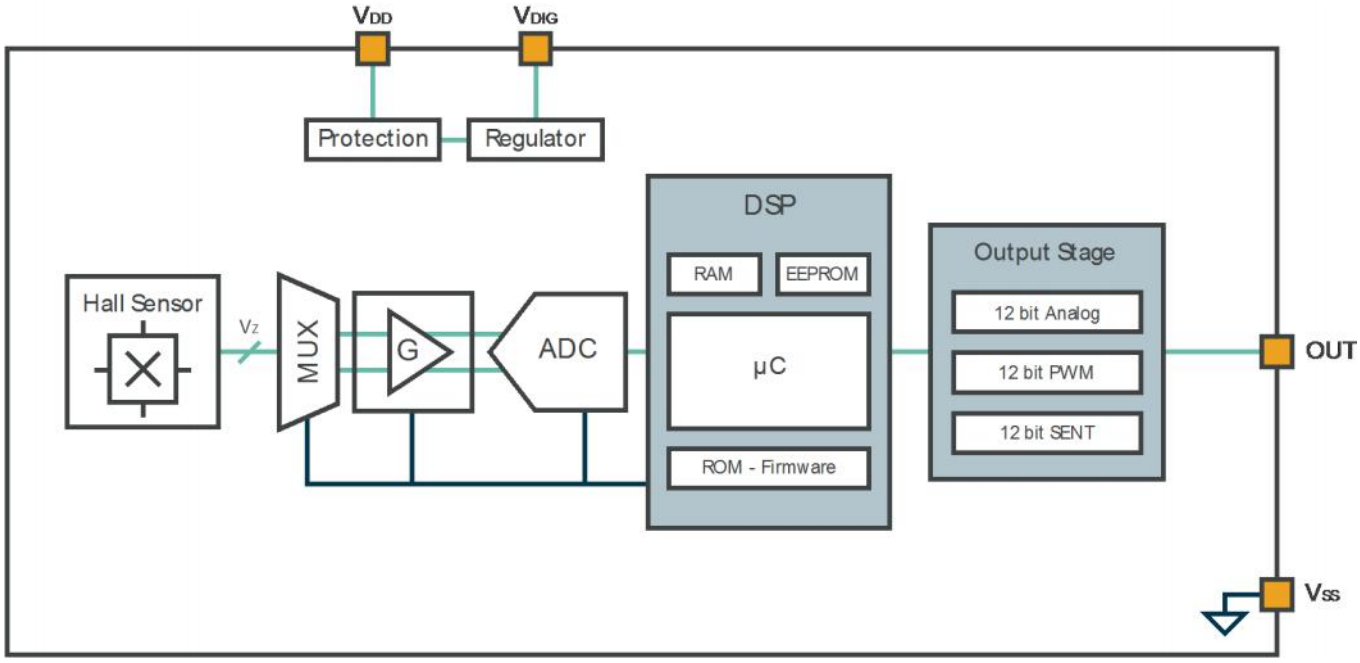


Figure 1 - Block Diagram

3. Glossary of Terms

Gauss (G), Tesla (T)	Units for the magnetic flux density - 1 mT = 10 G
TC	**T**emperature **C**oefficient (in ppm/Deg.C.)
NC	**N**ot **C**onnected
PWM	**P**ulse **W**idth **M**odulation
ADC	**A**nalog-to-**D**igital **C**onverter
LSB	**L**east **S**ignificant **B**it
MSB	**M**ost **S**ignificant **B**it
DNL	**D**ifferential **N**on-**L**inearity
INL	**I**ntegral **N**on-**L**inearity
RISC	**R**educed **I**nstruction **S**et **C**omputer
ASP	**A**nalog **S**ignal **P**rocessing
DSP	**D**igital **S**ignal **P**rocessing
ATAN	Trigonometric function: arctangent (or inverse tangent)
IMC	**I**ntegrated **M**agneto-**C**oncentrator (IMC®)
CoRDiC	**Co**ordinate **R**otation **Di**gital **C**omputer
	(i.e. iterative rectangular-to-polar transform)
EMC	**E**lectro-**M**agnetic **C**ompatibility
FE	**F**alling **E**dge
RE	**R**ising **E**dge
FW	**F**irmware
HW	**H**ardware
PWM	Pulse Width Modulation
%DC	Ratio Ton / Tperiod where Ton is the high state duration and Tperiod is the duration of 1 pwm period
MT3V	More than 3V Condition
MT4V	More than 4V Condition
LSD	Low Side Driver = Open drain N
PP	Push-Pull

Table 2 - Glossary of Terms

4. Pinout

PIN	SOIC-8	TSSOP-16
1	VDD	V_{DIG_1}
2	Test 0	V_{SS_1} ($Ground_1$)
3	Test 2	V_{DD_1}
4	Not Used	Test 0_1
5	OUT	Test 2_2
6	Test 1	OUT_2
7	VDIG	$Not\ Used_2$
8	VSS (Ground)	Test 1_2
9		V_{DIG_2}
10		V_{SS_2} ($Ground_2$)
11		V_{DD_2}
12		Test 0_2
13		Test 2_1
14		$Not\ Used_1$
15		OUT_1
16		Test 1_1

For optimal EMC behavior, it is recommended to connect the unused pins (Not Used and Test) to the Ground (see section 16).

5. Absolute Maximum Ratings

DC Operating Parameters at Nominal Supply Voltage (unless otherwise specified) and for Application Temperature Range T_A as specified by the Temperature Code.

Parameter	Value
Supply Voltage, VDD (overvoltage)	+ 24 V
Reverse Voltage Protection	– 12 V (breakdown at -14 V)
Positive Output Voltage	+ 18 V (breakdown at 24 V)
Output Current (IOUT)	+ 30 mA (in breakdown)
Reverse Output Voltage	– 0.3 V
Reverse Output Current	– 50 mA (in breakdown)
Operating Ambient Temperature Range, T_A	– 40 … + 150 Deg.C
Storage Temperature Range, T_S	– 40 … + 150 Deg.C
Magnetic Flux Density	± 1 T

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

6. Electrical Specification

DC Operating Parameters at Nominal Supply Voltage (unless otherwise specified) and for Application Temperature Range T_A as specified by the Temperature Code.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Nominal Supply Voltage	VDD		4.5	5	5.5	V
Supply Current[2]	IDD	Power saving Enabled		6	10[3]	mA
Isurge Current[4]	Isurge				20	mA
Power-On reset (rising)	HPOR_LH	Refer to internal voltage Vdig	2	2.25	2.5	V
Power-On reset Hysteresis	HPOR_Hyst		50		200	mV
Start-up Level (rising)	MT4V LH		3.8	4.0	4.2	V
Start-up Hysteresis	MT4V Hyst		50		200	mV
PTC Entry Level (rising)	MT7V_LH		5.8	6.2	6.6	V
PTC Entry Level Hysteresis	MT7V_Hyst		50		200	mV
Output Short Circuit Current	I_{short}	Vout = 0 V Vout = 5 V Vout = 18 V (T_A = 25Deg.C)			15 15 18	mA mA mA
Output Load	R_L	Pull-down to Ground Pull-up to 5V	4.7 4.7	10 10		kΩ kΩ
Analog Saturation Output Level	Vsat_lo	Pull-up load $R_L \geq 10$ kΩ to 5 V Pull-up load $R_L \geq 5$ kΩ to 18		0.5 2	2 3	%VDD
	Vsat_hi	Pull-down load $R_L \geq 5$ kΩ Pull-down load $R_L \geq 10$ kΩ	95 97.5	97 98.5		%VDD
Active Diagnostic Output Level	Diag_lo	Pull-up load $R_L \geq 10$ kΩ to 5 V Pull-up load $R_L \geq 5$ kΩ to 18V		0.5 2	2 3	%VDD
	Diag_hi	Pull-down load $R_L \geq 5$ kΩ Pull-down load $R_L \geq 10$ kΩ	95 97.5	97 98.5		%VDD
Passive Diagnostic Output Level (Broken Track Diagnostic) [5]	BVssPD	Broken Vss & Pull-down load $R_L \geq 5$ kΩ Pull-down load $R_L \geq 10$ kΩ	95 97.5			%VDD
	BVssPU	Broken Vss & Pull-up load $R_L \geq 1$kΩ	99.5	100		%VDD
	BVDDPD	Broken VDD & Pull-down load $R_L \geq 1$kΩ		0	0.5	%VDD
	BVDDPU	Broken VDD & Pull-up load $R_L \geq 5$kΩ			2	%VDD
Clamped Output Level	Clamp_lo	Programmable	0		100	%VDD[6]
	Clamp_hi	Programmable	0		100	%VDD[6]

2 For the dual version, the supply current is multiplied by 2.
3 To reach 10mA, the power saving option is enabled. This option switches off and on internal blocks dynamically. It can be disabled to reduce emission and meet stringent EMC requirements; the maximum supply current consumption then is increased up to 12mA.
4 The specified value is valid during early start-up time only; the current might dynamically exceed the specified value, shortly, during the Start-up phase.
5 For detailed information, see also section on Diagnostics
6 Clamping levels need to be considered vs the saturation of the output stage (see Vsat_lo and Vsat_hi)

As an illustration of the previous table, the MLX90293 fits the typical classification of the output span described on the Figure 2.

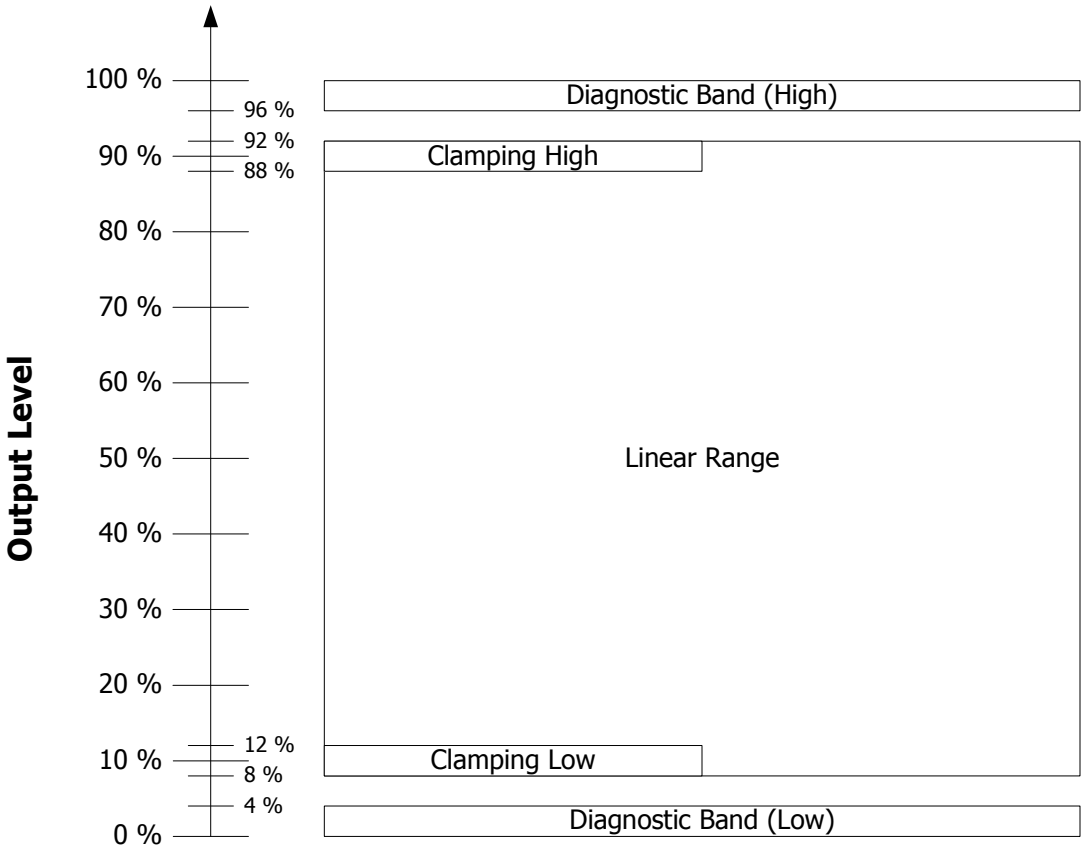


Figure 2 - Example of Output Span Classification for typical application

7. Isolation Specification

DC Operating Parameters at Nominal Supply Voltage (unless otherwise specified) and for Application Temperature Range T_A as specified by the Temperature Code. Only valid for the Package Code GO i.e. dual die version.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Isolation Resistance		Between dice	4			MΩ

8. Timing Specification

8.1. Generic Timings

DC Operating Parameters at Nominal Supply Voltage (unless otherwise specified) and for Application Temperature Range T_A as specified by the Temperature Code. These timings hold true regardless of the choosen communication protocol.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Main Clock Frequency	Ck	All contributors included thermal drift	12.6	13.3	14	MHz
Main Clock Frequency Thermal Drift	Δ^TCk				± 3%	Ck_{NOM}
Watchdog	Twd		114.5	118	121.5	ms

8.2. Timings in Analog/PWM mode

DC Operating Parameters at Nominal Supply Voltage (unless otherwise specified) and for Application Temperature Range T_A as specified by the Temperature Code.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Refresh Period	ts			441		µs
Latency over Refresh Period ratio		Filter=0[7] Filter=1 Filter=2 IIR is described separately in section 14.6		1.5 2 3		ts [refresh rate][8]
Start-up Cycle	Tsu	Analog OUT Slew-rate excluded			10	ms
Analog OUT Slew-rate		Mode 1 from C_{OUT} = 47 nF to 330 nF Mode 2: up to C_{OUT} = 10 nF Mode 3: up to C_{OUT} = 47 nF Mode 4: up to C_{OUT} = 330 nF	25 300 17 1.8	37 320 19 2.5		V/ms

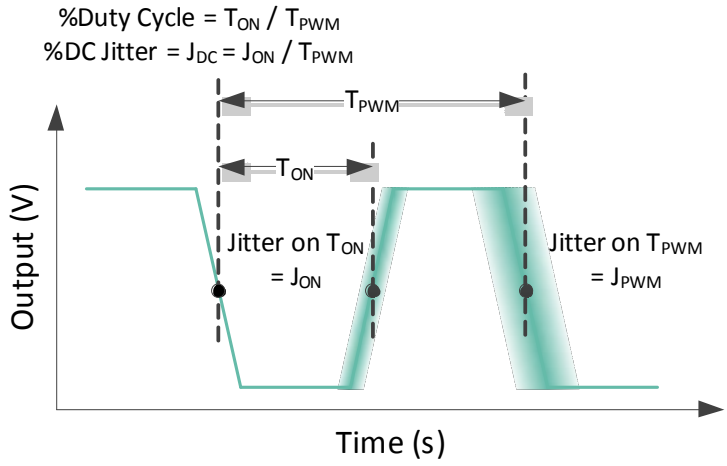
8.3. Timings specific for PWM Protocol

DC Operating Parameters at V_{DD} = V_{PU} = 5V (unless otherwise specified) and for T_A as specified by the Temperature Code.

7 See section 14.6 for details concerning Filter parameter
8 The step response time is the Refresh Period times ts. So, the step response time of filter = 1 is 882µs = 2x441 µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM Output Resolution	RPWM	12 bits		0.025		%DC/LSB
PWM % DC Jitter	JDC	LSD – Mode5 100Hz, 4.7nF, R_L = 1 kΩ PU 200Hz, 4.7nF, R_L = 1 kΩ PU 1000Hz, 4.7nF, R_L = 1 kΩ PU PP – Mode7 100Hz, 4.7nF, R_L = 1 kΩ PU 200Hz, 4.7nF, R_L = 1 kΩ PU 1000Hz, 4.7nF, R_L = 1 kΩ PU		 ±0.003 ±0.005 ±0.009 ±0.003 ±0.005 ±0.009	 ±0.016 ±0.02 ±0.035 ±0.016 ±0.02 ±0.035	%DC
PWM Freq Jitter	JPWM	LSD – Mode5 100-1000 Hz, 4.7nF, R_L = 1 kΩ PU PP – Mode7 100-1000 Hz, 4.7nF, R_L = 1 kΩ PU		±0.04 ±0.04	±0.15 ±0.15	Hz
PWM % DC thermal drift		LSD – Mode5 100Hz, 4.7nF, R_L = 1 kΩ PU 200Hz, 4.7nF, R_L = 1 kΩ PU 1000Hz, 4.7nF, R_L = 1 kΩ PU PP – Mode7 100Hz, 4.7nF, R_L = 1 kΩ PU 200Hz, 4.7nF, R_L = 1 kΩ PU 1000Hz, 4.7nF, R_L = 1 kΩ PU		 ±0.02 ±0.02 ±0.02 ±0.02 ±0.02 ±0.02	 ±0.03 ±0.03 ±0.05 ±0.03 ±0.03 ±0.05	%DC
PWM % DC Level drift (Trigger level= 25/50/75%)		LSD – Mode5 100Hz, 4.7nF, R_L = 1 kΩ PU PP – Mode7 100Hz, 4.7nF, R_L = 1 kΩ PU		±0.1 ±0.05	±0.15 ±0.1	%DC
PWM % DC Level drift		100Hz – PP Application Diagram (see below) Rs = 0, 50, 100, 150 Ohm Tolerance on R ± 20% Tolerance on C ± 30%		±0.05	±0.1	%DC

Jitter is defined by ± 3 σ for 1000 successive acquisitions with clamped output, see Figure below.



Parameter	Symbol	Test Conditions
PWM TON, TPWM	TON TPWM	Trigger level = 50 % Vpp
Rise time, Fall time		10% and 90% of amplitude
Jitter	JON JPWM	± 3 σ for 1000 successive acquisitions
Duty Cycle	% DC	TON / TPWM

Figure 3 - MLX90293 PWM measurement conditions.

8.4. Timings in SENT mode

DC Operating Parameters at Nominal Supply Voltage (unless otherwise specified) and for Application Temperature Range T_A as specified by the Temperature Code.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Tick time[9]		Ck = 13.3 MHz		3		µs
SENT Frame Period[10]	tframe	Ck = 13.3 MHz		882		µs
Maximal SENT Frame Tick Count[11] (pause pulse disabled)				256		ticks
Internal Measurement Period[12]	Tper	Ck = 13.3 MHz		441		µs
First Measurement to Sync Pulse latency	ta1	Ck = 13.3 MHz		1084		µs
Second Measurement to Sync Pulse latency	ta2	Ck = 13.3 MHz		643		µs
Latency (in case of Synchronous communication)	Latency	FILTER = 1 (recommended) SENT Transmission Included	1745	1745		µs
Start-up Time (up to first sync pulse)	tsu1			1.8		ms
Start-up Time (up to first data received)	tsu2	Last pause pulse not included		7.5	8.1	ms
Serial Message		Extended sequence (18 frames) Short sequence (8 frames)		15.9 7.1		ms ms
Rise Time @ Cable		Thresholds : 0.5V and 4.5V	3.0		5.3	µs
Rise Time @ Receiver			5.1		6.8	µs
Fall Time @ Cable			2.7		2.8	µs
Fall Time @ Receiver			4.8		4.9	µs

9 Tick time scales with Main Clock Frequency. Variation of Tick time for one IC is given by the Main Clock Frequency Thermal Drift.
10 This frame period with pause pulse enabled ensures synchronous communication. Synchronous means the time between data acquisition & signal transmitted in a SENT frame is fixed.
11 Length of frame depends on pause pulse enabled/disabled. The pause pulse and thus the frame length can be varied. A typical SENT frame is 56 ticks for the sync pulse, 8 nibble packages which vary between 12 & 25 ticks and an optional pause pulse which is at minimal 12 ticks.
12 This period is used if the pause pulse is enabled. If disabled, the Internal Measurement Period = 551µs, i.e. 25% higher.

8.5. Timing diagrams

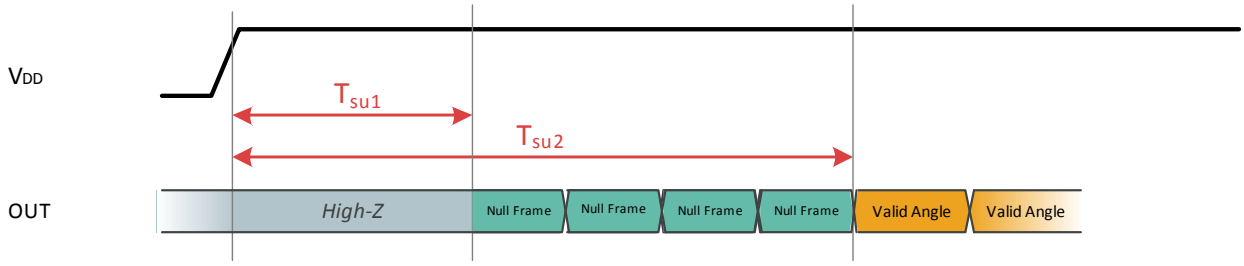


Figure 4 - Start-up phase timings

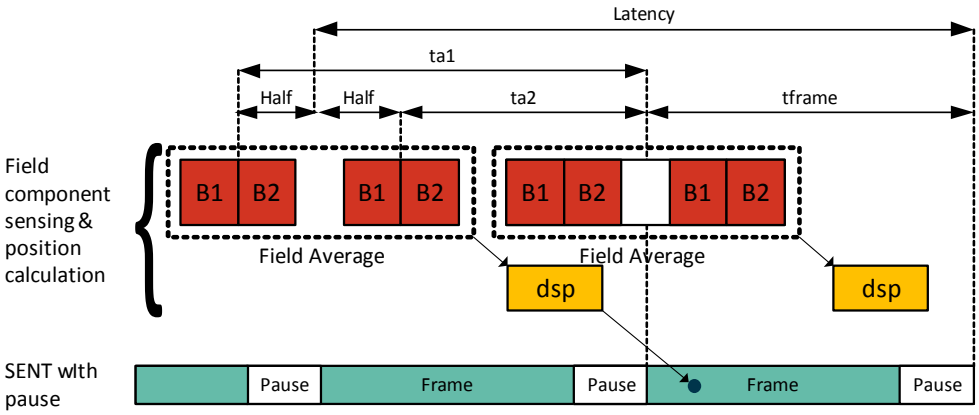


Figure 5 - Latencies (acquisition to output delays) – FILTER = 1 (recommended) Two readouts are averaged. Note: B1/B2 are needed to get one field readout.

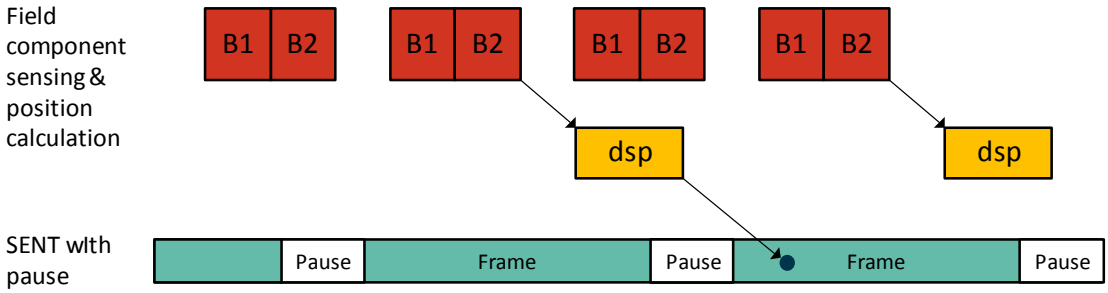


Figure 6 - Latency - Case FILTER = 0 (not recommended). The difference between Filter=0 & Filter =1 is that Filter =0 skips one acquisition of B1/B2.

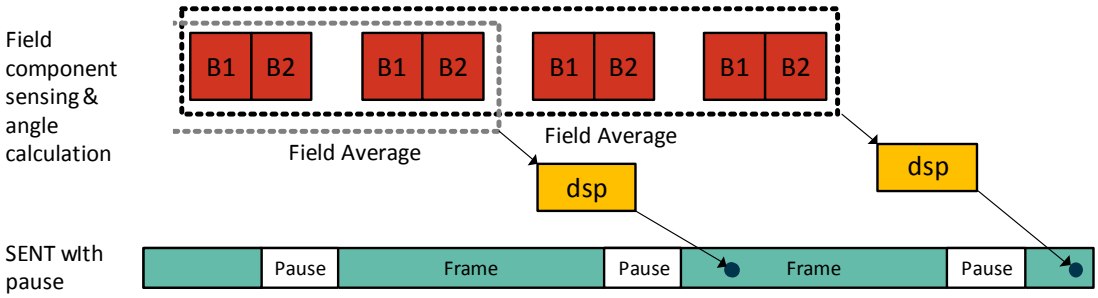


Figure 7 - Latency - Case FILTER = 2

8.6. Application diagram used for rise and fall time measurement

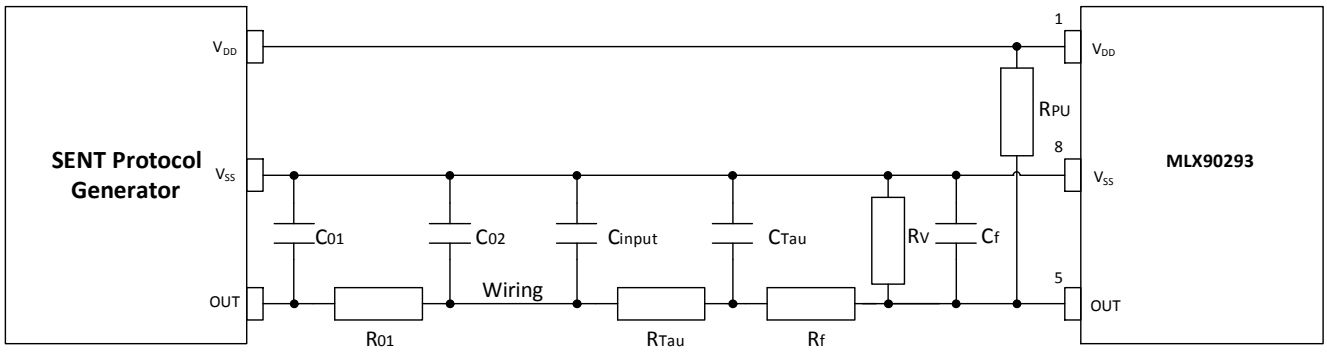


Figure 8 - Schematic used for rise and fall time measurements (ref: J2716 Rev Jan 2010 Fig. 6.3.4)

Component	Value	Unit
C_{01}	10 ± 25%	nF
C_{02}	not mounted	nF
R_{01}	not mounted	Ω
C_{input}	68	pF
C_{Tau}	2.2	nF
C_f	100	pF
R_{Tau}	568	Ω
R_f	10	kΩ
R_{PU}	14.7	kΩ
R_V	not mounted	Ω

Component values used for rise and fall time measurements (ref: J2716 Rev Jan 2010 Fig. 6.3.4)

9. Accuracy specification

DC Operating Parameters at Nominal Supply Voltage (unless otherwise specified) and for Application Temperature Range T_A as specified by the Temperature Code.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ADC Resolution on the raw signals				15		bits
Thermal Offset Drift	$\Delta^T V_{OQ}$	Without system compensation	-0.45[13] -0.35		0.45 0.35	%Span
Analog Output Resolution	R_{DAC}	12b DAC (Theoretical, Noise free) INL (before EOL calibration) DNL	-4 0.05	0.025 1	+4 3	%VDD/ LSB12
Output stage Noise		Clamped Output		0.05	0.075	%VDD
Overall Noise[14]	3σ	EE_VG = 21 (=span of 30mT)			0.1	%VDD
Ratiometry Error [15]		4.5V ≤ VDD ≤ 5.5V LT4V ≤ VDD ≤ MT7V	-0.05 -0.1		+0.05 +0.1	%VDD
Sensitivity Drift[16]	$\Delta^T S$	Intrinsic IC Sensitivity Drift (Temperature Code=L)	-190		190	ppm/Deg.C
Sensitivity Drift[16]	$\Delta^T S$	Intrinsic IC Sensitivity Drift (Temperature Code=E)	-150		150	ppm/Deg.C

10. Magnetic Specification

DC Operating Parameters at Nominal Supply Voltage (unless otherwise specified) and for Application Temperature Range T_A as specified by the Temperature Code.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Magnetic Flux Density	B_Z		-150		150	mT
Magnet Temperature Coefficient [17]	TCm		-4000		0	ppm/Deg.C

11. CPU & Memory Specification

The DSP is based on a 16 bit RISC µController. This CPU provides 2.5 Mips while running at 10 MHz.

13 Parts with lowered thermal offset drift are available. A thermal offset drift within [-0.45%,0.45%] is ordered with MLX90293Exx-ADM-0xx-xx. A thermal offset drift within [-0.35%, 0.35%] is ordered with MLX90293Exx-ADM-1xx-xx.
14 Noise pk-pk (peak-to-peak) is 3 sigma Noise. The application diagram used is described in the recommended wiring. For detailed information, refer to section Filter in application mode (Section 14). This specification is achieved with Hard Filter & IIR filter k=4 while meeting a response time of <1ms
15 Analog output only
16 Lifetime include
17 See also section 14.2

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ROM				10		KB
RAM				384		B
EEPROM				128		B

12. Traceability Information

Every device contains a unique ID that is programmed by Melexis in the EEPROM. Melexis strongly recommends storing this value during the EOL (End-Of-Line) programming to ensure full traceability of the final product.

These parameters shall never be erased during the EOL programming.

Parameter	Comments	Default Values	Parameter # bit
MELEXISID1	Melexis identification reference	MLX	16
MELEXISID2	Melexis identification reference	MLX	16
MELEXISID3	Melexis identification reference	MLX	16

13. End-User Programmable Items

Parameter	Function or Comment	Default	Remark
EE_VG	Analog Gain[18]	14h	Default : analog gain = 20
EE_OSMOD	Output stage configuration	F4h	(19)
EE_USERCFG0	User configuration 0	00h	(19)
EE_USERCFG1	User configuration 1	A2h For Zx; depends on field direction	(19)
EE_USERCFG2	User configuration 2	00h	(19)
EE_CALIBMODE_L	Calibration coefficients	00h	Enables extreme thermal compensation scaling(19)
EE_SERIAL_ID_1 / EE_PWMTL	ID of user serial message #1 / PWM period lsbyte	D0h	(20)
EE_SERIAL_ID_2 / EE_PWMTH	ID of user serial message #2 / PWM period msbyte	07h	(20)
EE_SERIAL_ID_3 / EE_PWMDC	ID of user serial message #3 / PWM duty cycle (when in fault reporting mode)	00	
EE_SERIAL_ID_4	ID of user serial message #4	0x00	
EE_SSYS12	{EE_Ssys2, EE_Ssys1}	00h	Signed 2's complement(21)
EE_SSYS35	{EE_Ssys5, EE_Ssys3}	00h	(21)
EE_SSYS67	{EE_Ssys7, EE_Ssys6}	00h	(21)

18 The setting of the analog gain must be done in order to prevent ADC saturation that can lead to a measurement error, please contact Melexis. See also ADC Clipping section15
19 See section 14.1.1
20 See section 14.1.2
21 See section 14.2.5

Parameter	Function or Comment	Default	Remark
EE_SERIAL_DATA_1 / OSYS12	User SENT serial data / {EE_OSYS2, EE_OSYS1}	0000h	If Sent serial messages are used, piecewise linear compensation cannot be used for the system's offset drift and vice versa. System sensitivity drift is always available. The IC is optimized by Melexis to reduce IC offset & sensitivity drift[22]
EE_SERIAL_DATA_2 / OSYS35	User SENT serial data / {EE_OSYS3, EE_OSYS5}	0000h	
EE_SERIAL_DATA_3 / OSYS67	User SENT serial data / {EE_OSYS6, EE_OSYS7}	0000h	
EE_SERIAL_DATA_4 / IIR_K	Data of user serial message #4	0000h	EE_SERIAL_DATA_4 or IIR_K[23] if FILTER[19]=3
EE_DIGOFFSETIN	Digital offset enabling pre-scaling at start of customer DSP	E0h	Signed word[24]
EE_DIGGAININ	Digital gain enabling scaling at start of customer DSP	10h	Unsigned word[24]
EE_BPIVOT	Customer pivot point for temperature compensation (Byte)	80h	50% output span[25]
EE_LNR_ Y0	Y coordinate point 0/16	0000h	-50% output span[25]
EE_LNR_ Y1	Y coordinate point 1/16	1000h	[25]
EE_LNR_ Y2	Y coordinate point 2/16	2000h	[25]
EE_LNR_ Y3	Y coordinate point 3/16	3000h	[25]
EE_LNR_ Y4	Y coordinate point 4/16	4000h	[25]
EE_LNR_ Y5	Y coordinate point 5/16	5000h	[25]
EE_LNR_ Y6	Y coordinate point 6/16	6000h	[25]
EE_LNR_ Y7	Y coordinate point 7/16	7000h	[25]
EE_LNR_ Y8	Y coordinate point 8/16	8000h	[25]
EE_LNR_ Y9	Y coordinate point 9/16	9000h	[25]
EE_LNR_ Y10	Y coordinate point 10/16	A000h	[25]
EE_LNR_ Y11	Y coordinate point 11/16	B000h	[25]
EE_LNR_ Y12	Y coordinate point 12/16	C000h	[25]
EE_LNR_Y13	Y coordinate point 13/16	D000h	[25]
EE_LNR_Y14	Y coordinate point 14/16	E000h	[25]
EE_LNR_Y15	Y coordinate point 15/16	F000h	[25]
EE_LNR_Y16	Y coordinate point 16/16	FFFFh	150% output span[25]
EE_CLAMPLOW	Clamping Low	8000h	50%[25]
EE_CLAMPHIGH	Clamping High	8000h	50%[25]
EE_DIGOFFSETOUT	Digital offset enabling scaling in the customer DSP	00h	Signed word[24]

22 See section 14.2.4
23 See section 14.6.2
24 See section 14.2.2
25 See section 14.2.3

Parameter	Function or Comment	Default	Remark
EE_DIGGAINOUT	Digital gain enabling scaling at start of customer DSP	04h	Unsigned word DIGGAINOUT & DIGOFFSETOUT shall not be changed unless a unipolar application where maxField / minField < 2. Contact Melexis in this case.(24)
EE_SENT_SERIAL	SENT sequence options	08h	Use User Interface to correctly set this parameter.(26)
EE_ROMCHECKSUM/ EE_HARDTHRESHOLD	ROM checksum (when patch is used) Hard Threshold (when hard threshold is enabled) Enabled ROM checksum with patch & Hard Threshold are mutually exclusive	20h	Checksum can be skipped with word EE_CRC_DISABLE
EE_SENT_CFG	{EE_PRESCALER_N[3:0], EE_PRESCALER_M[3:0]}	2Ah	
EE_USERID1	User ID1	0000h	(27)
EE_USERID2	User ID2	0000h	(27)
EE_USERID3	User ID3	0000h	(27)
EE_DIAG_SETTINGS	Diagnostics options	0088h	(26)

Melexis strongly recommends checking the User Identification data (Parameters USERID) during EOL programming.

14. Description of End-User Programmable Items

14.1. Output modes

14.1.1. Out mode

- EE_OSMOD determines the Output Stage (Analog, digital, high-impedance, SENT). A distinction is being made between normal operation & start-up or fault.

EE_OSMOD							
B7	B6	B5	B4	B3	B2	B1	B0
OS_DIAG.DIAG	OS_DIAG.MODE[2:0]			x	OS_NORM.MODE[2:0]		

OS_DIAG.MODE[2:0] defines the mode when there is a fault, or when in start-up. In all other cases, the output stage is defined by OS_NORM.MODE[2:0].

26 See section 14.3.2
27 See section 14.3.3

OS_NORM.MODE[2:0]	Type	Descriptions	Comments
0	Not used	Not used	
1	Analog	Analog Rail-to-Rail for Coutmin = 47nF	Analog Only
2	Analog	Analog Rail-to-Rail for Coutmax = 10nF	Analog Only
3	Analog	Analog Rail-to-Rail for Coutmax = 68nF	Analog Only
4	Analog	Analog Rail-to-Rail for Coutmax = 330nF	Analog Only
5	Digital	open drain NMOS	PWM
6	Digital	open drain PMOS	PWM
7	Digital	Push-Pull	PWM/SENT

OS_DIAG.DIAG determines the reporting level (diagnostic low, diagnostic high) during start-up (both analog and PWM mode), or during a fault reporting (Only in Analog mode).

- Enabling SENT or PWM requires selecting the appropriate Output Stage and enabling the appropriate bit in EE_USERCFG0. The parameter is defined in the table below.

Byte	Bit	Function
EE_USERCFG0	0	Melexis internal
	1	SENT
	2	PWM
	3	PWMPOL
	4	PWMSLEWRATE
	5	TREATSEQ[0]
	6	TREATSEQ[1]
	7	POLARITY
EE_USERCFG1	0	MAPXYZ[0]
	1	MAPXYZ[1]
	2	FILTER[0]
	3	FILTER[1]
	4	Select_Sent_Osys
	5	SENT_pause_nibbleout
	6	DAC output sign
	7	EnableHardThreshold
EE_USERCFG2	0	Melexis internal
	1	Melexis internal
	2	Melexis internal
	3	free
	4	MEMLOCK[0]
	5	MEMLOCK[1]
	6	Melexis internal
	7	Melexis internal
EE_CALIBMODE_L	0	OutputScaling : scale the output from a span from -50% to 150% output span if True. Otherwise, from 0% to 100% (default : False)
	3	Ssys2xSpan. The magnet thermal compensation SSYS coefficient goes from [0.5, 1.496] if true. Otherwise, it go from [0.75, 1.248] (default : False)

14.1.2. PWM Output Mode

If PWM output mode is selected, the output signal is a digital signal with Pulse Width Modulation (PWM). The PWM polarity is selected by the PWMPOL parameter (see section 14.1.1):

- PWMPOL = 1 for a low level at 100%
- PWMPOL = 0 for a high level at 100%

The PWM frequency is selected by EE_PWMTL and EE_PWMTH parameters. The following table provides typical code for different target PWM frequency and for both low and high speed modes.

PWM F (Hz)	PWMT (LSB) @13.3MHz	PWM res. (µs)	PWM res. (%)	PWM res. (bit)
100	44333	0.240	0.0024	15
250	17733	0.240	0.006	14
500	8866	0.240	0.012	13
1000	4433	0.240	0.024	12

Notes:

- A more accurate trimming can be performed to take into account initial tolerance of the main clock.
- The PWM frequency is subjected to the same tolerances as the main clock (see ΔTCk).

14.2. Output Transfer Characteristic

14.2.1. Introduction

The main focus of this chapter is the correction over position.

The transfer from magnetic field to output can be optimized by the customer. In the MLX90293ADM, the following three compensation mechanisms have been implemented:

- Piecewise linear compensation of the **thermal sensitivity drift**. A correction factor for the sensitivity can be defined at 7 equidistant temperature points between -50degC and 160degC. Values at other points are linearly interpolated. The parameter names are EE_Ssys1 up to EE_Ssys7.
- Piecewise linear compensation of the **thermal offset drift**. A correction value for the offset drift can be defined at 7 equidistant temperature points between -50degC and 160degC. Values at other points are linearly interpolated. The parameter names are EE_Osys1 up to EE_Osys7.
- Piecewise linear compensation **over position** (LNR): A value for the desired output can be defined at 17 equidistant magnetic points. The implementation works in two steps:
  - First, the input for the LNR function is achieved by ‘stretching’ the input signal. Here, the two parameters EE_DIGGAININ & EE_DIGOFFSETIN are used
  - Next, the compensation is achieved by the 17 parameters EE_LNR_ Y0 up to EE_LNR_Y16.

The remainder of this chapter assumes the reader knows the following three concepts:

- Signed parameters are in two’s complement
- The Digital Signal Processing chain usually calculates with 16 bit numbers. For example, the final compensated digital signal is a value from 0 up to 65535. Any deviation from this rule will be highlighted.
- The following parameter naming convention is used throughout the chapter. Every output of one calculation is the input for the next step, see also next section 14.2.2.

- B1 = input field which comes after the analog to digital converter (Melexis only)
- B2 = signal after Hall-Element Offset compensation (Melexis only)
- B3 = signal after Hall-Element Sensitivity compensation (Melexis only)
- B4 = signal data after Polarity and Filter functions (Melexis only) (=B_IC_TC)
- B5a = signal after digital offset and gain functions (customer programmable)
- B7 = signal after system sensitivity compensation (customer programmable)
- B6 = signal after system offset compensation output (customer programmable)
- B5b= signal after the piecewise linear compensation over position (customer programmable)
- B8 = signal after scaling (Melexis only) (=B_SYS_TC)
- B9 = signal after clamping (customer programmable)
- B10 = signal for DAC, PWM or SENT (protocol is customer programmable)

14.2.2. Order selection of the calculation

A user can select the order of customer selectable calculations. The following table shows the possible sequences. To select, please use the parameter TREATSEQ (see EE_USERCFG0 in section 14.1.1).

TREATSEQ[1:0]=0	TREATSEQ[1:0]=1	TREATSEQ[1:0]=2	TREATSEQ[1:0]=3
1. Hall Offset(T)	1. Hall Offset(T)	1. Hall Offset(T)	1. Hall Offset(T)
2. Hall Sens(T)	2. Hall Sens(T)	2. Hall Sens(T)	2. Hall Sens(T)
3. Polarity	3. Polarity	3. Polarity	3. Polarity
4. Filters	4. Filters	4. Filters	4. Filters
5a. Apply Pre-scaling	5a. Apply Pre-scaling	5a. Apply Pre-scaling	5a. Apply Pre-scaling
5b. LNR	6. System Offset(T)	5b. LNR	7. System Sens(T)
6. System Offset(T)	7. System Sens(T)	7. System Sens(T)	6. System Offset(T)
7. System Sens(T)	8a. Post scaling	6. System Offset(T)	8a. Post scaling
8b. 2x Scaling	5b. LNR	8a. Post scaling	5b. LNR
8a. Post scaling	8b. 2x Scaling	8b. 2x Scaling	8b. 2x Scaling
9. Clampings	9. Clampings	9. Clampings	9. Clampings
10. DAC Map	10. DAC Map	10. DAC Map	10. DAC Map

Important: please refer to OutputScaling (see EE_CALIBMODE_L in 14.1.1) as this is Post scaling. Apply Pre-scaling uses digital gain and offset with EE_DIGOFFSETIN & EE_DIGGAININ whereas Post Scaling uses EE_DIGOFFSETOUT & EE_DIGGAINOUT. Users can also enable/disable 8b. 2x Scaling.

14.2.3. Piecewise Linear Compensation over Position

The LNR parameters (EE_LNR_ Y0, … EE_LNR_ Y16, and EE_BPIVOT), together with the clamping values (EE_CLAMPLOW and EE_CLAMPHIGH), fully define the relation (the transfer function) between the digital angle and the output signal.

The shape of the MLX90293 transfer function from the digital angle value to the output voltage is described by the drawing below. In the 16 segments mode, the output transfer characteristic is Piece-Wise-Linear (PWL).

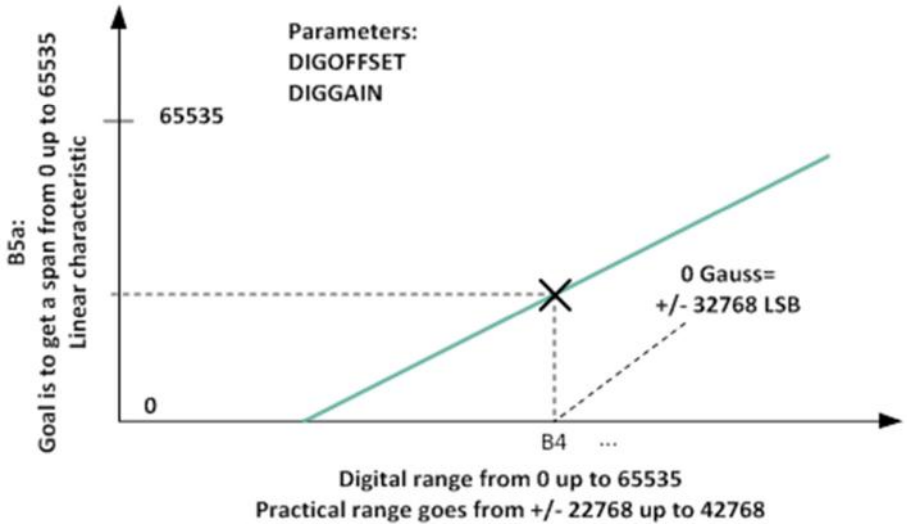


Figure 9a - The input from the analog chain is scaled to ensure a good input range for the piecewise linear compensation in (b)

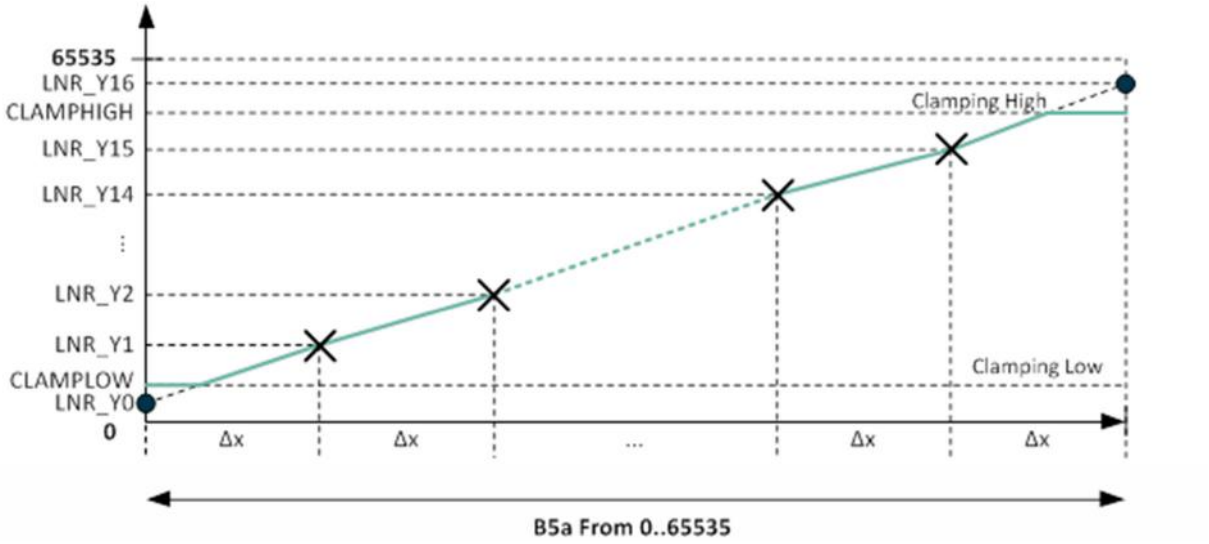


Figure 9b - Input range from 65.5Deg. up to 360Deg.

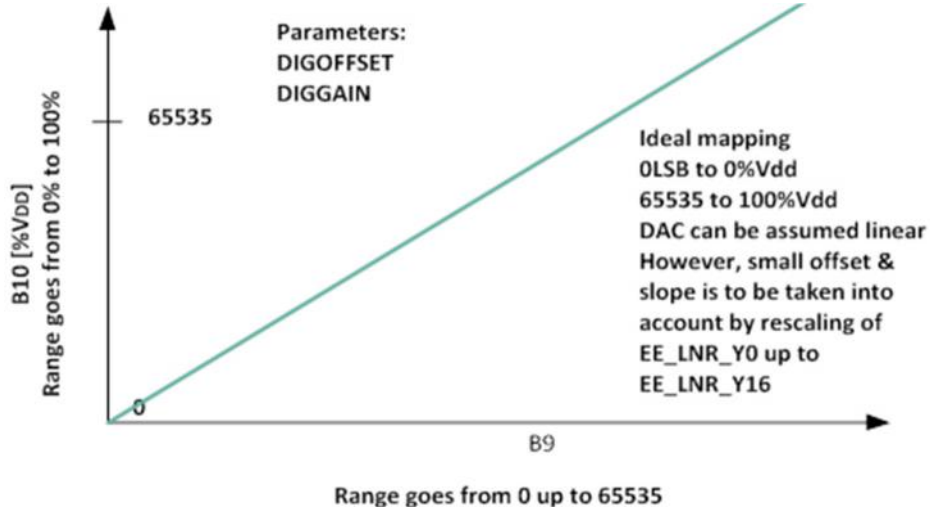


Figure 9c - The OUTPUT4DAC is transformed to an analog output.

Figure 9 (a,b,c) - The graphs show the transfer characteristic of each of the customer configurable parameters.

IMPORTANT: customer who only needs a linear relation between magnetic field & output will only deal with EE_DIGGAINx & EE_DIGOFFSETx (x=IN or OUT).

The sequence for customer to trim for piecewise linear compensation over position is depicted here:

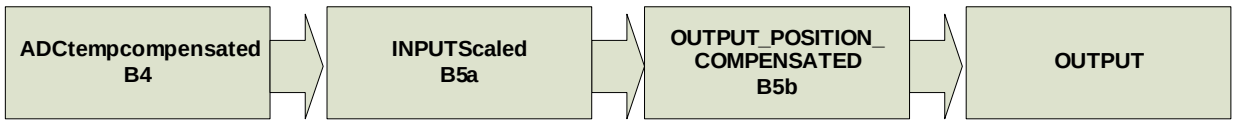


Figure 10 - The following sequence is to be trimmed by customers to enable piecewise linear compensation.

To trim parts, the following steps & equations have to be followed.

Step1: Select the Analog Gain code VG

To minimize the quantization errors occurring at the A/D converter, one shall select the highest possible analog gain, and one shall use the digital gain capability to trim the circuit sensitivity in a fine manner.

Step2: trim the scaling factors EE_DIGGAINx & EE_DIGOFFSETx (x=IN or OUT)

$$B5a = (B4 – EE\_DIGOFFSETx*2^8) * EE\_DIGGAINx*2^8 / 2^{10}$$

The following equation is to be used by customers to ensure the span of B5a goes from 0 up to 65535.

Step3: trim the piecewise linear coefficients EE_LNR_ Y0, … EE_LNR_ Y16

These coefficients determine the desired output for the 17 equidistant input points. See Figure 9b). Thus, customers program the desired output for these 17 points. The intermediate points come from a linear interpolation.

Value for LNRY	Output
0	-50%Vdd
65535	150%Vdd

14.2.4. Piecewise Linear Compensation for Thermal Offset Drift

Customers can trim the system offset drift. The IC's intrinsic offset drift is minimized by Melexis. If you intend to use thermal offset drift for the system –not IC-, please contact Melexis.

This functionality is only available if customer set the parameter EE_USERCFG1[4]= Select_Sent_Osys to 0 (default). Then, the 3 first EEPROM words are used for system offset compensation. Otherwise, the EEPROM content for EE_OSYS1 up to EE_OSYS7 can be (optionally) used for SENT communication. Also, the transfer equation also depends on the order defined in section 14.2.2.

Osys(Tlin) = (PWL_7(Tlin) / 256) * 32, PWL_7 stands for piecewise linear compensation.

The output Osys(Tlin) is added to the input value.

Here, Tlin goes from -50degC up to 160degC. The values in the EEPROM are defined in the next table. Tlin is the temperature as measured by the IC.

Value for LNRY	EEPROM parameter
PWL_7(Tlin=-50degC)	EE_OSYS1
PWL_7(Tlin=-15degC)	EE_OSYS2
…	…
PWL_7(Tlin=125degC)	EE_OSYS6
PWL_7(Tlin=160degC)	EE_OSYS7

14.2.5. Piecewise Linear Compensation for Thermal Sensitivity Drift

Customers can trim the system's sensitivity drift. The IC's intrinsic sensitivity drift is minimized by Melexis. The Melexis tooling helps to minimize the system thermal drift caused by for example, the magnet thermal drift.

The transfer equation also depends on the order defined in section 14.2.2.

Ssys (Tlin) = (2^{15} + PWL_7(Tlin) / 256 * 128) if EE_CALIBMODE_L[3]=1, otherwise Ssys (Tlin) = (2^{15} + PWL_7(Tlin) / 256 * 64). PWL_7 stands for piecewise linear compensation. The former enables a correction span from [0.75, 1.248], the latter from [0.5, 1.496].

The output Ssys(Tlin)/ 2^{15} shows the relative sensitivity change for a given IC temperature Tlin.

Here, Tlin goes from -50degC up to 160degC. The values in the EEPROM are defined in the next table. Tlin is the temperature as measured by the IC.

Value for LNRY	EEPROM parameter
PWL_7(Tlin=-50degC)	EE_SSYS1
PWL_7(Tlin=-15degC)	EE_SSYS2
…	…
PWL_7(Tlin=125degC)	EE_SSYS6
PWL_7(Tlin=160degC)	EE_SSYS7

14.2.6. CLAMPING Parameters

The clamping levels are two independent values to limit the output voltage range. The EE_CLAMPLOW parameter adjusts the minimum output voltage level. The EE_CLAMPHIGH parameter sets the maximum output voltage level. Both parameters have 16 bits of adjustment and are available for both LNR modes. In analog mode, the resolution will be limited by the D/A converter (12 bits) to 0.024%VDD. In PWM mode, the resolution will be 0.024%DC.

14.3. SENT output Protocol

14.3.1. Generalities

The MLX90293 complies with the sub-set "**A.3 Single Secure Sensors**" of the norm J2716 Revised **JAN2010**.

Remark: A customer has to select either piecewise linear compensation of the offset drift (zero gauss point) or the SENT serial message.

14.3.2. Single Secure Fast Channel

MLX90293 delivers SENT frames according the Single Secure format. This format is explicitly described in this section.

- Frame Content

The 90293 SENT frames have 6 data nibbles, and are formatted according the below table.

SENT frame								
Status[0:3]	D1-MSN	D1-MidN	D1-LSN	D2-MSN	D2-MidN	D2-LSN	CRC	Optional pause

Where the corresponding frame contents are defined in the table below:

Content	description
Status[0]	Channel 1 indicator ("1"= error,"0" otherwise) (see section 14.3.2)
Status[1]	0
Status[2]	Enhanced serial Message (see section 14.3.3)
Status[3]	Enhanced serial Message (see section 14.3.3)
CRC	Enhanced CRC (the legacy CRC is not featured)
D1	Position
D2-MSN	D2-MSN = Rolling Counter - MSN
D2-MidN	D2-MidN = Rolling Counter - MidN
D2-LSN	D2-LSN = Inverted copy of D1-LSN
Pause pulse	Pause pulse when activated (see section 14.3.2)

Note: To minimize frame length, the value of the rolling counter can be forced to zero. Overwrite ForceCntrZero (see EE_SENT_SERIAL below).

Byte	Bit	Function	
EE_SENT_SERIAL	0	EE_CODE_REPORT[0]	EE_CODE_REPORT[2:0] controls how diagnostic are reported in channel 1: Channel1 = 4088 + EE_CODE_REPORT[2:0] when in diagnostic and EE_CODE_REPORT>0 Channel1 = output value always when EE_CODE_REPORT=0.
	1	EE_CODE_REPORT[1]	
	2	EE_CODE_REPORT[2]	
	3	ForceCntrZero	ForceCntrZero. in case of True, counter in SENT frame is set to 0 to reduce message length.
	4	Reserved	
	5	Reserved	
	6	EE_EXTENDEDSEQUENCE	EE_EXTENDEDSEQUENCE=1 enables the long sequence of slow messages.
	7	Not used - 0	

- Diagnostic Reporting through the fast channel

Diagnostic Reporting, bit Status[0]

The bit Status[0] is high whenever the three following conditions are met:

1. A diagnostic (analog/environmental) detects an error[28]

2. The reporting of the above error is enabled[29]

3. The debouncing time has elapsed.

Diagnostic Reporting, Channel 1

The diagnostic can be reported through the 12 bit payload of channel 1, and not only through the status bit Status[0]. The EEPROM parameters EE_CODE_REPORT[2:0] controls the diagnostic reporting through channel 1 as follow:

If EE_CODE_REPORT[2:0]=0, the channel 1 reports the angle, and not the diagnostic, as if no diagnostic.

The error is reported only thanks to the Status bits.

---

28 A diagnostic of type digital cause the circuit to switch in fail-safe-mode
29 See EEPROM bits EE_DIAG_SETTINGS

If EE_CODE_REPORT[2:0]>0, the channel1 payload contains the value Channel1 = (4088 + EE_CODE_REPORT[2:0])

Diagnostic Reporting Time

The Diagnostic Reporting Time is programmable (defined as multiple of a macro-cycle unit time).

A macro-cycle is a sequence of 20 angle acquisitions, and has a duration of approximately 6 ms.

Diagnostic Debouncing

The Diagnostic Reporting is debounced. The debouncing paramater are user-programmable, by steps of approximately 6 ms.

Pause pulse

A pause pulse, as defined by the standard, is present at the end of every frame. The pause pulse mode can be disabled. Please contact our local Melexis representative to obtain the complete procedure for deactivating the pause pulse mode. The pause pulse is adjusted by the circuit so that the frame period is constant.

The field sensing and the frame synchro pulse are in sync.

Fast Channel CRC

The 90293 features the new recommended implementation.

14.3.3. Slow Channel

- Enhanced Serial Message

The circuit encodes the slow messages according the Enhanced Serial Message Format as specified at Chapter 5.2.4.3 of the SENT norm, except for the following restriction:

The configuration bit is always 0, meaning that the payload consists in 12-bit data and 8-bit message ID.

- Serial Message Sequence

The circuit complies with the following sub-set specifications of the norm for pressure sensors

(The norm for the angular sensor case does not specify the serial message format)

#	8bit ID	Item	12 bit data	Comments
1	29	Sensor ID	Prog.	EE_USERID1_12LSB
2	01	Error Code	RAM	Described in section 14.3.3
3	2A	Sensor ID	Prog.	{EE_USERID2_8LSB, EE_USERID1_4MSB }
4	01 / 80	Error Code / User-defined RAM value	RAM	RAM variable @ address EE_RAM_PROBE_ADDR e.g. Temp, GainCode, FieldStrength
5	2B	Sensor ID	Prog.	{EE_USERID3_4LSB,EE_USERID2_8 MSB}
6	01	Error Code	RAM	
7	2C	Sensor ID	Prog.	EE_USERID3_12MSB
8	01 / 80	Error Code / User-defined RAM value	RAM	RAM variable @ address EE_RAM_PROBE_ADDR e.g. Temp, GainCode, FieldStrength

#	8bit ID	Item	12 bit data	Comments
Optional Part (EE_ExtendedSequence = 1)				
9	06	SENT Revision	003	
10	01	Error Code	RAM	
11	EE_SERIAL_ID1	User-defined #1	EE_SERIAL_DATA_1	e.g. Sensor type, Manufacturing code
12	01 / 80	Error Code / User-defined RAM value	RAM	RAM variable @ address EE_RAM_PROBE_ADDR e.g. Temp, GainCode, FieldStrength
13	EE_SERIAL_ID12	User-defined #2	EE_SERIAL_DATA_2	e.g. 07 – Kennlinie
14	01	Error Code	RAM	
15	EE_SERIAL_ID3	User-defined #3	EE_SERIAL_DATA_3	e.g. 03 – Sensor Type
16	01 / 80	Error Code / User-defined RAM value	RAM	RAM variable @ address EE_RAM_PROBE_ADDR e.g. Temp, GainCode, FieldStrength
17	EE_SERIAL_ID4	User-defined #4	EE_SERIAL_DATA_4	
18	01	Error Code	RAM	

The first part (positions 1 to 8) provides the Error Code and the Sensor ID alternatively. The second part (positions 9 to 18) is optional as a whole enabled with EEPROM bit (EE_ExtendedSequence=1[30]). This second part consists in the error code (5 occurrences), 4 User-defined messages (ID and data) and the SENT revision.

The temperature can be derived from user-defined RAM value (see below), with the following equation:
User-defined RAM value = 8 * (Tlin[C] – 35[C]) + 865 LSB12 when User-defined RAM value= ramTempSens
The accuracy of the actual Temperature is around ± 10 Deg.C.

Serial message sequence period

Sequence Length (serial message count)	Sequence Length (frame count)	Sequence Period (ms, typical)
8	144	121
18	324	273

User-defined RAM Value

The payloads of the positions 4, 8 (and 12, 16 if relevant) are user-defined. Three possibilities:

- Error Code
- 12 LSB of a user-defined RAM value
- 12 MSB of a user-defined RAM value
- The positions 4, 12, 16, 20 refer to the same user-defined RAM address.

Thus, customers may choose to send the user-defined RAM Values of the following parameter.

Variable name	Address	Description
ramTempSens	42	Temperature sensor value

30 See EE_SENT_SERIAL in section 14.3.2

Error Code Rate

The Error Code are on purpose transmitted every second message, to maximize the rate, which equals then 36 SENT frames, when the user-defined RAM mode is not enabled (72 otherwise).

- Serial Message Error Code

The Serial error code contains the error

Bit position	Diagnostic	Comments
3	ADCSatura	Diagnostic
4	ADCMonitor	ADC monitor
5	VanaMoni	Analog Internal Supply Too Low
6	VddMoni	External Supply Too Low, Too High
7	Rough Offset	Front-end Rough Offset too low, too high
8	TempMonitor	Temperature Sensor monitor

14.3.4. Start-up

During the chip initialization the output remains high until the circuit emits four initialization frames (all 6 data nibble zero). The fifth frame is not an initialization frame but a valid frame containing a measured angle.

See also the section 8, “Timing Specification”.

14.3.5. Field sensing (A2D conversions) and the frame Synchro pulse

The digital output value (fast channel payload) results of the average of two values. These values are themselves computed from 4 ADCs values.

The time between the ADCs and the frame synchro pulse is constant. As a result the phase delay between the magnetic field value and the SENT synchro pulse is constant, allowing filtering at the ECU side.

See also section 8, “Timing Specification”.

14.4. Identification

Parameter	Value
EE_USERID1	0…65535
EE_USERID2	0…65535
EE_USERID3	0…65535

Identification number: 48 bits (3 words) freely useable by Customer for traceability purpose.

14.5. Lock

The MEMLOCK write protects all the EEPROM parameters set by the Melexis and user[31]. Once the lock is enabled, it is not possible to change the EEPROM values anymore.

Note that the Memlock bits should be set by the solver function “MemLock".

31 See EE_USERCFG2 in section 14.1.1

14.6. Digital Filter

14.6.1. Introduction

The MLX90293ADM offers both a Finite Impulse Response Filter and an Infinite Impulse Response Filter. Here, IIR filters are considered better for closed loped systems as these have a smaller parasitic phase delay. To enable extreme noise reduction, customers can also combine an IIR filter with a hard threshold.

14.6.2. Specification & EEPROM settings

The table below gives the response time of the different filters for a step change.

Filter Type	Relative Noise Reduction Factor	Phase Delay (#samples)	90% Response Delay vs No Filter (#samples)
No filter	1	0	Δ = 0
FIR(1,1)	1:0.707	0.5	Δ = 0
FIR (1,1,1,1)	1:0.500	1.5	Δ = 3
IIR_K=2,	1:0.578	< 1	Δ = 3
IIR_K=2.66,	1:0.480	0 . 1.6	Δ = 4
IIR_K=4	1:0.379	< 3	Δ = 7

See the table below how the minimal step change is defined in case of a hard threshold.

EEPROM parameter	Description	EEPROM value	comment
FILTER[32] (2b)	No filter	0	
	FIR(1,1)	1	
	FIR (1,1,1,1)	2	
	1st order IIR	3	Can be combined with Hard Threshold. Important, set also IIR_K
IIR_K([33]) (2b)	k=2	8000h	IIR filter where k is used for transfer function $y_n=y_{n-1}+(x_n-y_{n-1})/k$ Filter = (1<<16)
	k=2.66	603E	
	k=4	4000	
	k=8	2000	
	k=16	1000	

14.6.3. Hard Threshold

The hard threshold enables bypassing the IIR filter during a fast field change. This field change is a user definable threshold called “Hard Threshold”. This setting is recommended in applications where strong filtering is beneficial and where immediate response is wanted during extreme position changes of the sensor. However, this behaviour is non linear, so careful testing is recommended if this setting is used in a closed feedback system.

Using this feature requires enabling EnableHardThreshold[32] and setting the value for the parameter Hard Threshold. To define, measure the noise of B_IC_TC at a fixed position under normal operation. Then, the 6 times the standard deviation of this signal’s variation will determine the hard threshold value.

32 See EE_USERCFG1 in section 14.1.1
33 See section 13

14.7. Programmable Diagnostic Settings

14.7.1. DIAG mode

Defines the Output Stage mode in case of Diag.

OS_DIAG.mode [2:0]	Type	Descriptions	Comments
0	Disable	Output HiZ	Not recommended
5	Digital	open drain NMOS	
6	Digital	open drain PMOS	
7	Digital	Push-Pull	

14.7.2. DIAG Level

Determines the reporting level (diagnostic low, diagnostic high) during start-up (both analog and PWM mode), or during a fault reporting (Only in Analog mode).

In PWM mode, the fault reporting level shall in principle be 0 when the leading edge is a rising edge, (resp. 1 for a falling edge) in order to detect the first cycle after start-up. MLX recommends then DIAG Level = PWMPOL.

14.7.3. Diagnostic Features

It is recommended to enable the diagnostic features for safety critical applications. See section 15.

14.8. EEPROM endurance

Although the EEPROM is used for Calibration Data Storage (similarly to an OTPROM), the MLX90293 embedded EEPROM is qualified to guarantee an endurance of minimum 1000 write cycles at 125˚C for (engineering/calibration purpose).

15. Self Diagnostic

The MLX90293 provides numerous self-diagnostic features. Those features increase the robustness of the IC functionality as it will prevent the IC to provide erroneous output signal in case of internal or external failure modes ("fail-safe").

Diagnostic Item	Action	Effect on Outputs	Type	Monitoring Rate	Reporting Rate
Start-up phase Diagnostics					
RAM March C-10N Test	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic low/ high Reporting (optional)	Digi HW	n/applicable (start-up only)	n/applicable (start-up only)
Watchdog BIST	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic low/ high Reporting (optional)	Digi HW	n/applicable (start-up only)	n/applicable (start-up only)
Under Voltage Monitoring *SUPPLYMONI = (MT3VB) OR (MT4VB)*	Start-up on Hold ** ** CPU reset after 120ms	Diagnostic low/high	Environ &Analog	n/applicable (start-up only)	n/applicable (start-up only)
Over Voltage Monitoring *MT7V*	PTC entry	Output in High-Impedance	Environ	n/applicable (start-up only)	n/applicable (start-up only)
Back-Ground Loop Diagnostics					
ROM 16bit checksum (continuous)	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic low//high Reporting (optional)	Digi HW	$80 \cdot DTI_{DIG}$	$80 \cdot DTI_{DIG}$
EEPROM 8 bit CRC Check (continuous)	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic low/high Reporting (optional)	Digi HW	$1 \cdot DTI_{DIG}$	$1 \cdot DTI_{DIG}$
Watchdog (continuous)	CPU reset	--	Digi HW	120ms	n/a
DSP Loop Diagnostics					
ADC Clipping ADCCLIP[34]	Debouncing (programmable)	SENT Status bit0 = 1 (optional)	Environ &Analog	5/DSP	$DTIANA \times \frac{Diag\_Debounce\_Thresh}{Diag\_Debounce\_Stepup}$
ADC Monitor (Analog to Digital Converter) *ADCMONI*	Debouncing (programmable)	SENT Status bit0 = 1 (optional)	Analog HW	1/DSP	$DTIANA \times \frac{Diag\_Debounce\_Thresh}{Diag\_Debounce\_Stepup}$

34 Diagnostic disabled per default. In order to reach the diagnostic coverage as described in the safety manual, this diagnostic needs to be enabled after completing the setting of the analog gain, see footnote 18. Please contact Melexis for more information.

Diagnostic Item	Action	Effect on Outputs	Type	Monitoring Rate	Reporting Rate
Under Voltage Monitoring *SUPPLYMONI = (MT3VB) OR (MT4VB)*	Supply Debouncing (programmable)	SENT Status bit0 = 1 (optional)	Environ &Analog	1/DSP	$\text{DTIANA} \times \frac{\text{Diag\_Debounce\_Thresh}}{\text{Diag\_Debounce\_Stepup}}$
Over Voltage Monitoring *MT7V*	PTC entry after PTC Debouncing	Output in High-Impedance	Environ	$8/20 \cdot DTI_{ANA}$	$8/20 \cdot DTI_{ANA}$
Temperature Sensor Monitor *TEMPMONI*	Debouncing (programmable)	SENT Status bit0 = 1 (optional)	Analog	1/DSP	$\text{DTIANA} \times \frac{\text{Diag\_Debounce\_Thresh}}{\text{Diag\_Debounce\_Stepup}}$
Hardware Diagnostics (continuously checked by dedicated Logic)					
Read/Write Access out of physical memory	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic Low/High	Digi HW	n/a immediate Diag	n/a immediate Diagnostic
Write Access to protected area (IO and RAM Words)	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic low/high	Digi HW	n/a immediate Diag.	n/a immediate Diagnostic
Unauthorized Mode Entry	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic low/high	Digi HW	n/a immediate Diag	n/a immediate Diagnostic
EEPROM Error Correcting Code (Hamming correction)	(Transparent) Error Correction	No effect	Digi HW	n/a.	n/a
Hardware Diagnostics (continuously checked by dedicated Analog circuits)					
Broken VSS	CPU Reset on recovery	Pull down load => Diagnostic High Pull up load => Diagnostic High	Environ	n/a immediate Diagnostic	n/a immediate Diagnostic
Broken V_{DD}	CPU Reset on recovery	Pull down load => Diagnostic Low Pull up load => Diagnostic Low	Environ	n/a immediate Diagnostic	n/a immediate Diagnostic
Resistive Cable Test	Start-up on Hold	Diagnostic low/high	Environ	n/a immediate Diagnostic	n/a immediate Diagnostic.

Dimension	Min	Typ	Max	Unit
DTI_{ANA}	5.7	6.0	6.3	ms
DTI_{DIG}	3.9	7.2	10[(35)]	ms

Table 3 - Timing Specification @13.16 MHz

35 DTIDIG (eg. 10ms worst case) Corresponds to 20 output refresh time (eg. 500µs)

16. Recommended Application Diagrams

16.1. MLX90293 in SOIC-8 Package

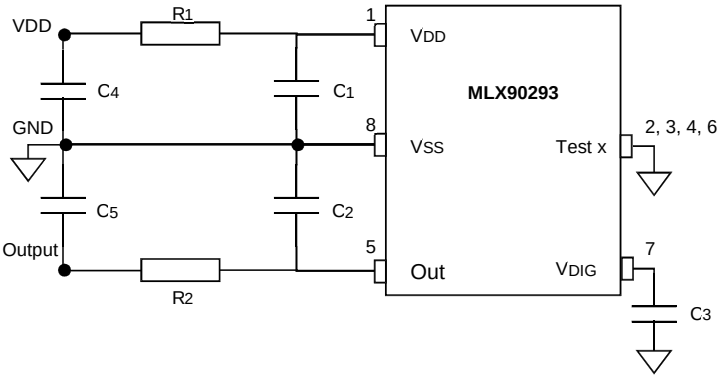


Figure 11 – Recommended wiring for the MLX90293 in SOIC-8 package

Output	Compact PCB routing			EMC robust PCB routing			
Analog Output	Min	Typ.	Max	Min	Typ.	Max	Remarks
C1	100 nF	100 nF	1 uF	47 nF	100 nF	1 uF	Close to the pin
C2 (20)	47 nF	100 nF	330 nF	47 nF	100 nF	330 nF	Close to the pin
C3	47 nF	100 nF	220 nF	47 nF	100 nF	220 nF	Close to the pin
C4	-	-	-	500 pF	1 nF	10 nF	Connector Side
C5	-	-	-	500 pF	1 nF	10 nF	Connector Side
R1	-	-	-	0 Ω	10 Ω	33 Ω	Increased ratiometry error
R2	-	-	-	10 Ω	50 Ω	100 Ω	

Table 4 - Recommended capacitances for the MLX90293 in analog output mode for SOIC-8 package

Output	Compact PCB routing			EMC robust PCB routing			
PWM Output	Min	Typ.	Max	Min	Typ.	Max	Remarks
C1	100 nF	100 nF	1 uF	47 nF	100 nF	1 uF	Close to the pin
C2	2.2 nF	4.7 nF	22 nF	2.2 nF	4.7 nF	22 nF	Close to the pin
C3	47 nF	100 nF	220 nF	47 nF	100 nF	220 nF	Close to the pin
C4	-	-	-	500 pF	1 nF	10 nF	Connector Side
C5	-	-	-	500 pF	1 nF	2.2 nF	Connector Side
R1	-	-	-	0 Ω	10 Ω	33 Ω	Impacts the Voltage on VDD pin
R2	-	-	-	10 Ω	50 Ω	100 Ω	

Table 5 - Recommended capacitances for the MLX90293 in PWM mode for SOIC-8 package

Output	Compact PCB routing			EMC robust PCB routing			
SENT	Min	Typ.	Max	Min	Typ.	Max	Remarks
C1	100 nF	100 nF	1 uF	47 nF	100 nF	1 uF	Close to the pin
C2	2.2 nF	4.7 nF	22 nF	2.2 nF	4.7 nF	22 nF	Close to the pin
C3	47 nF	100 nF	220 nF	47 nF	100 nF	220 nF	Close to the pin
C4	-	-	-	500 pF	1 nF	10 nF	Connector Side
C5	-	-	-	500 pF	1 nF	2.2 nF	Connector Side
R1	-	-	-	0 Ω	10 Ω	33 Ω	Impacts the Voltage on VDD pin
R2	-	-	-	10 Ω	50 Ω	100 Ω	

Table 6 - Recommended capacitances for the MLX90293 in SENT mode for SOIC-8 package

16.2. MLX90293 in TSSOP-16 Package

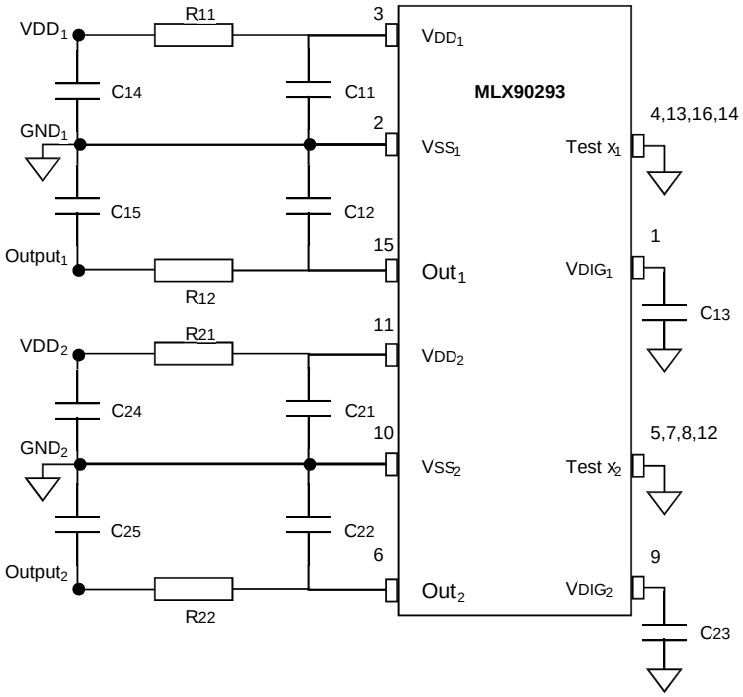


Figure 12 – Recommended wiring for the MLX90293 in TSSOP-16 package

Output	Compact PCB routing			EMC robust PCB routing			
Analog Output	Min	Typ.	Max	Min	Typ.	Max	Remarks
C11, C21	100 nF	100 nF	1 uF	47 nF	100 nF	1 uF	Close to the pin
C12, C22	47 nF	100 nF	330 nF	47 nF	100 nF	330 nF	Close to the pin
C13, C23	47 nF	100 nF	220 nF	47 nF	100 nF	220 nF	Close to the pin
C14, C24	-	-	-	500 pF	1 nF	10 nF	Connector Side
C15, C25	-	-	-	500 pF	1 nF	10 nF	Connector Side
R11, R21	-	-	-	0 Ω	10 Ω	33 Ω	Increased ratiometry error
R12, R22	-	-	-	10 Ω	50 Ω	100 Ω	

Table 7 - Recommended capacitances for the MLX90293 in ANALOG mode for TSSOP-16 package

Output	Compact PCB routing			EMC robust PCB routing			
PWM Output	Min	Typ.	Max	Min	Typ.	Max	Remarks
C11, C21	100 nF	100 nF	1 uF	47 nF	100 nF	1 uF	Close to the pin
C12, C22	2.2 nF	4.7 nF	22 nF	2.2 nF	4.7 nF	22 nF	Close to the pin
C13, C23	47 nF	100 nF	220 nF	47 nF	100 nF	220 nF	Close to the pin
C14, C24	-	-	-	500 pF	1 nF	10 nF	Connector Side
C15, C25	-	-	-	500 pF	1 nF	2.2 nF	Connector Side
R11, R21	-	-	-	0 Ω	10 Ω	33 Ω	Impacts the Voltage on VDD pin
R12, R22	-	-	-	10 Ω	50 Ω	100 Ω	

Table 8 - Recommended capacitances for the MLX90293 in PWM mode for TSSOP-16 package

Output	Compact PCB routing			EMC robust PCB routing			
SENT Output	Min	Typ.	Max	Min	Typ.	Max	Remarks
C11, C21	100 nF	100 nF	1 uF	47 nF	100 nF	1 uF	Close to the pin
C12, C22	22 nF	4.7 nF	22 nF	2.2 nF	4.7 nF	22 nF	Close to the pin
C13, C23	47 nF	100 nF	220 nF	47 nF	100 nF	220 nF	Close to the pin
C14, C24	-	-	-	500 pF	1 nF	10 nF	Connector Side
C15, C25	-	-	-	500 pF	1 nF	2.2 nF	Connector Side
R11, R21	-	-	-	0 Ω	10 Ω	33 Ω	Impacts the Voltage on VDD pin
R12, R22	-	-	-	10 Ω	50 Ω	100 Ω	

Table 9 - Recommended capacitances for the MLX90293 in SENT mode for TSSOP-16 package

17. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to standards in place in Semiconductor industry.

For further details about test method references and for compliance verification of selected soldering method for product integration, Melexis recommends reviewing on our web site the General Guidelines soldering recommendation. For all soldering technologies deviating from the one mentioned in above document (regarding peak temperature, temperature gradient, temperature profile etc), additional classification and qualification tests have to be agreed upon with Melexis.

For package technology embedding trim and form post-delivery capability, Melexis recommends to consult the dedicated trim&form recommendation application note: lead trimming and forming recommendations

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/en/quality-environment

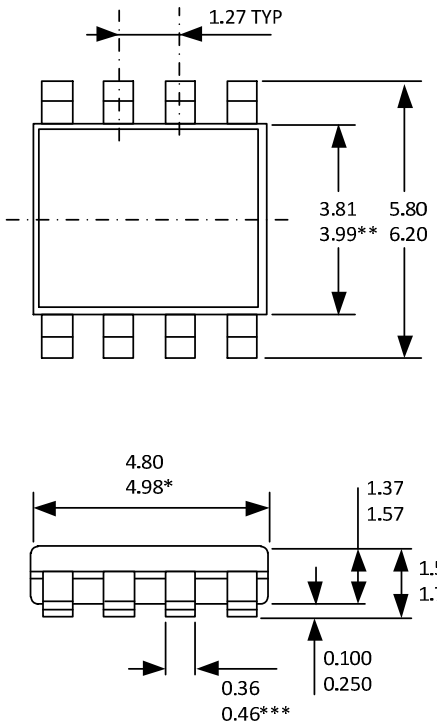
18. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).

Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

19. Package Information

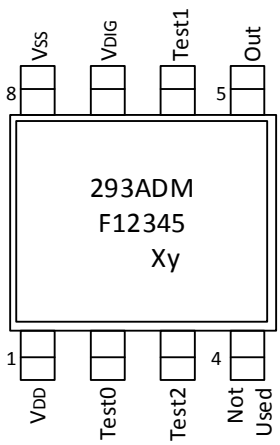
19.1. SOIC-8 - Package Dimensions



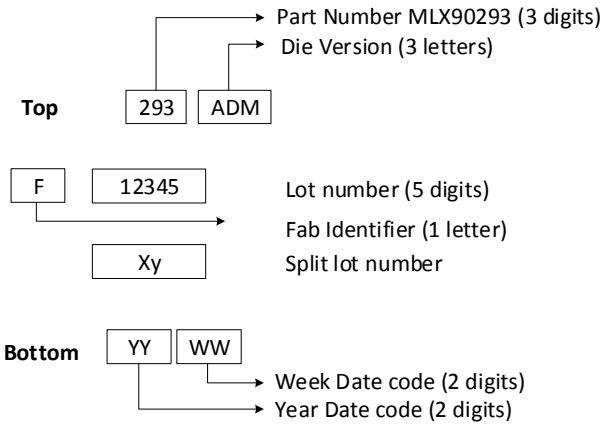
NOTES:

All dimensions are in millimeters (angles in degrees).
* Dimension does not include mold flash, protrusions or gate burrs (shall not exceed 0.15 per side).
** Dimension does not include interleads flash or protrusion (shall not exceed 0.25 per side).
*** Dimension does not include dambar protrusion.
Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition.
Dambar cannot be located on the lower radius of the foot.

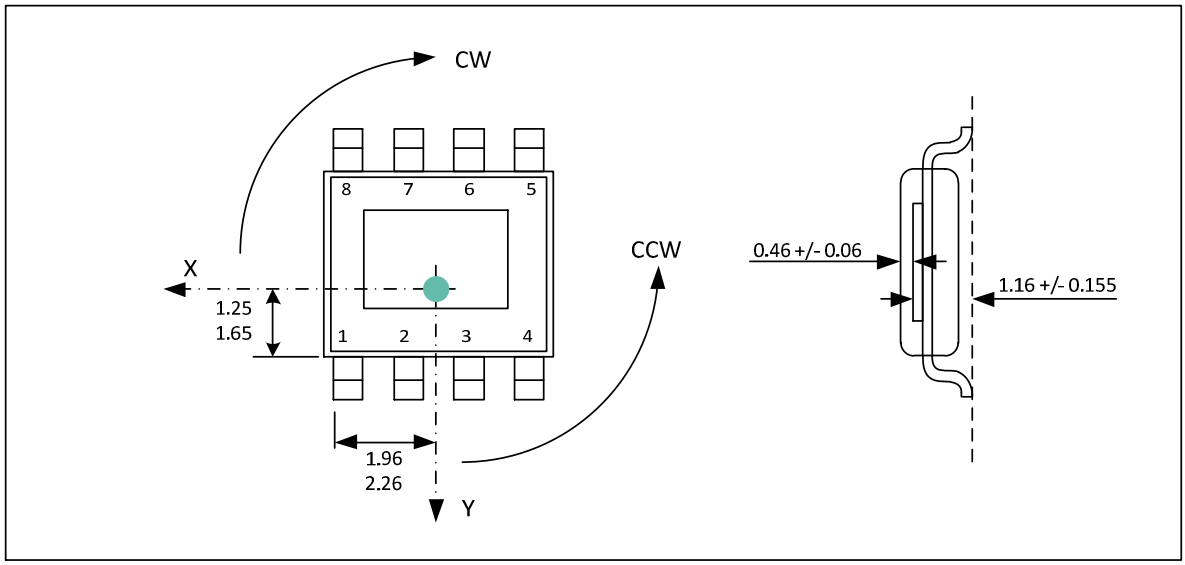
19.2. SOIC-8 - Pinout and Marking



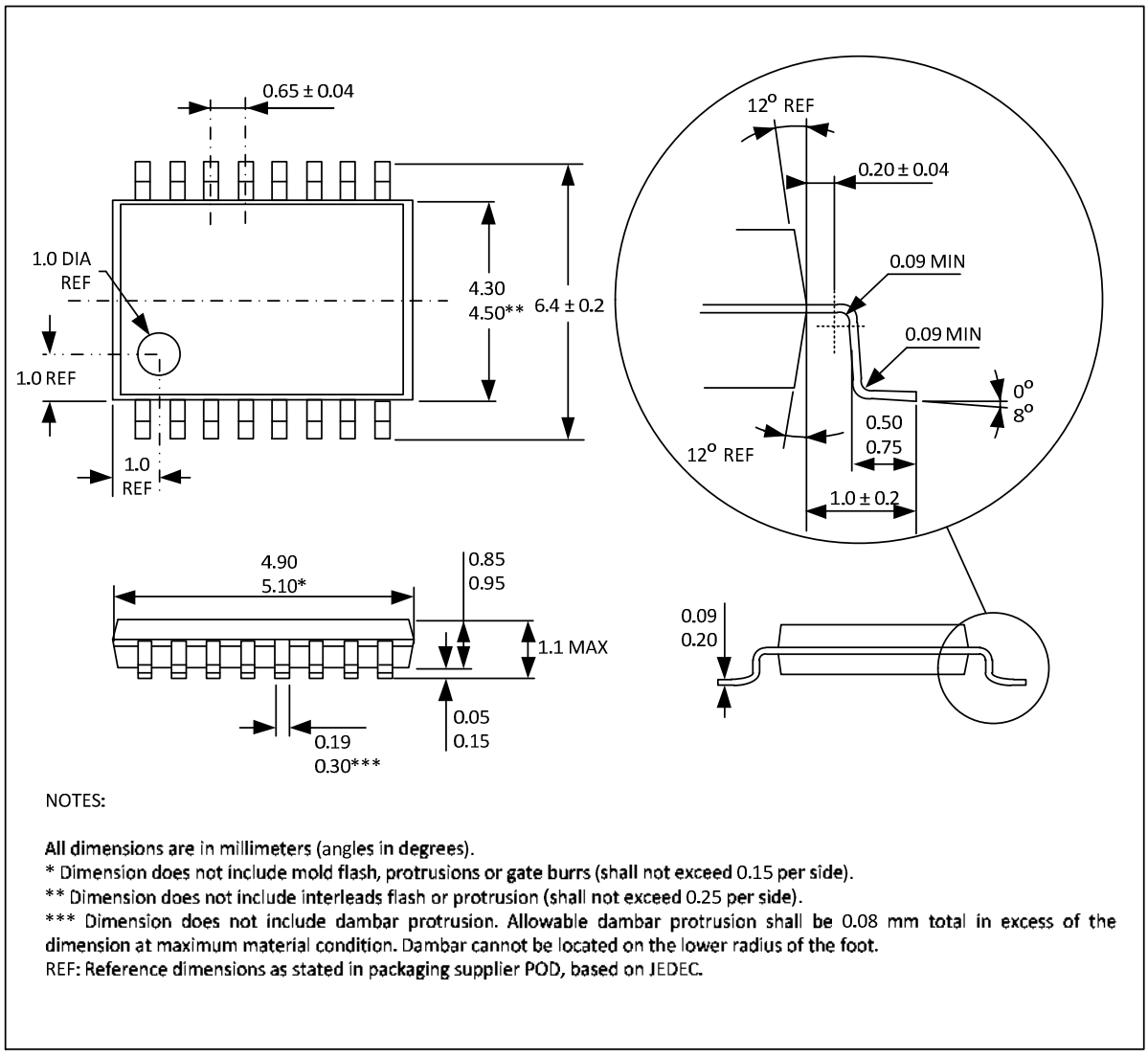
Marking :



19.3. SOIC-8 - Sensitive spot positioning



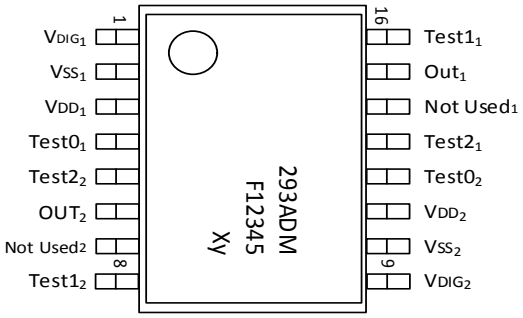
19.4. TSSOP-16 - Package Dimensions

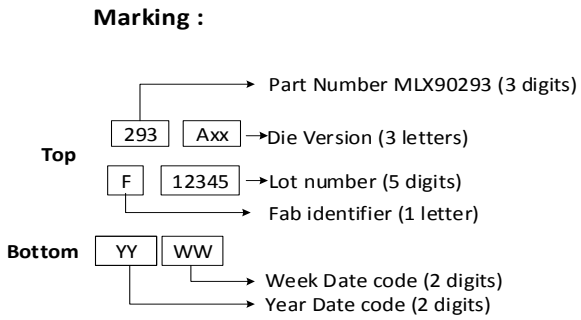


NOTES:

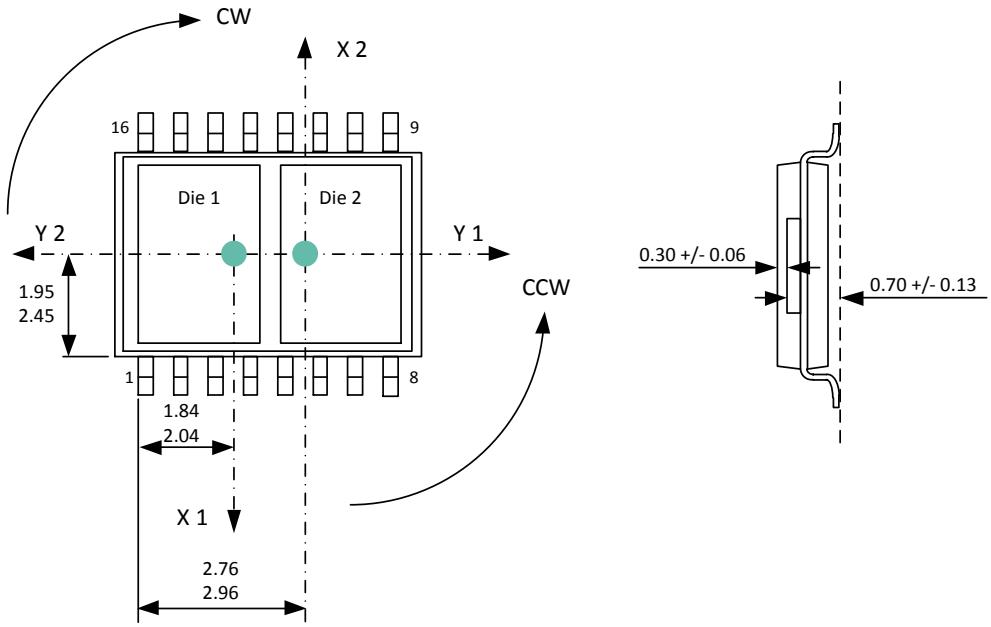
All dimensions are in millimeters (angles in degrees).
* Dimension does not include mold flash, protrusions or gate burrs (shall not exceed 0.15 per side).
** Dimension does not include interleads flash or protrusion (shall not exceed 0.25 per side).
*** Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.
REF: Reference dimensions as stated in packaging supplier POD, based on JEDEC.

19.5. TSSOP-16 - Pinout and Marking





19.6. TSSOP-16 - Sensitive spot positioning



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