NOVOSENSE

NSI822xC

High Reliability Dual-Channel Digital Isolators

Datasheet (EN) 1.4

Product Overview

The NSI822xC devices are high reliability dual-channel digital isolators. The NSI822xC device is safety certified by UL1577 support several insulation withstand voltages (3.75kVrms, 5kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI822xC is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/us. The NSI822xC device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI822xC device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Key Features

- Up to 5000V_{rms} Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 250kV/us
- Chip level ESD: HBM: ±8kV
- Robust EMC Reinforced Dual-Channel Digital Isolators for SOW8 wide body and SOW16 wide body
- Default output high level or low level option
- Isolation surge voltage: >10kV
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
    - SOP8 narrow body
    - SOW8 wide body
    - SOW16 wide body

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

Part Number	*Package*	*Body Size*
NSI822xCx-DSPR	SOP8	4.90mm × 3.90mm
NSI822xCx-DSWVR	SOW8	5.85mm × 7.50mm
NSI822xCx-DSWR	SOW16	10.30mm × 7.50mm

Functional Block Diagrams

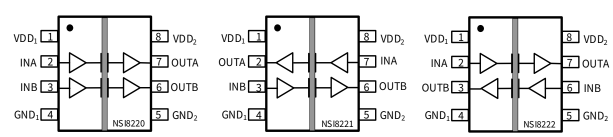

Figure 1. NSI822xC SOP8 Block Diagram

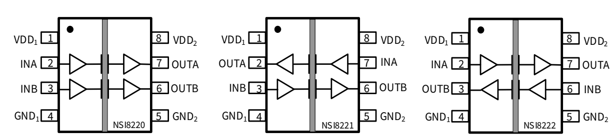

Figure 2. NSI822xC SOW8 Block Diagram

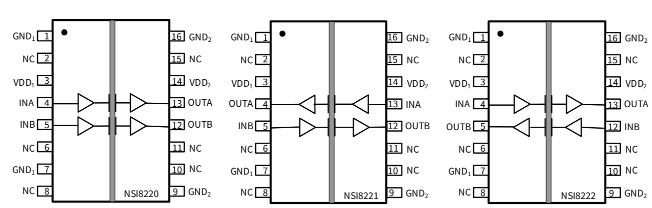

Figure 3. NSI822xC SOW16 Block Diagram

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1. Pin Configuration and Functions

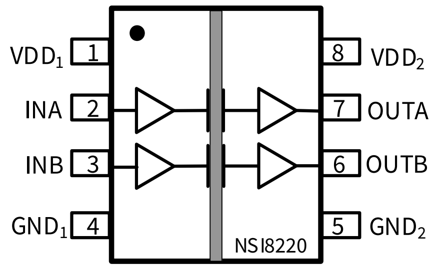


Figure 1.1 NSI8220Cx SOP8 Package

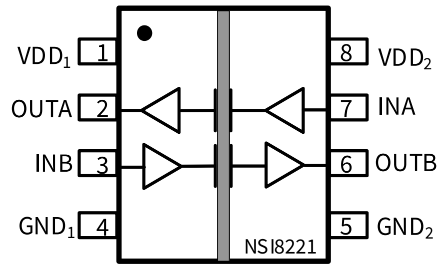


Figure 1.2 NSI8221Cx SOP8 Package

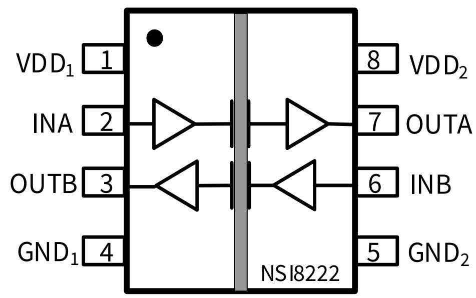


Figure 1.3 NSI8222Cx SOP8 Package

Table1.1 NSI8220C/ NSI8221C/ NSI8222C SOP8 Pin Configuration and Description

NSI8220C PIN NO.	NSI8221C PIN NO.	NSI8222C PIN NO.	SYMBOL	FUNCTION
1	1	1	VDD1	Power Supply for Isolator Side 1
2	7	2	INA	Logic Input A
3	3	6	INB	Logic Input B
4	4	4	GND1	Ground 1, the ground reference for Isolator Side 1
5	5	5	GND2	Ground 2, the ground reference for Isolator Side 2
6	6	3	OUTB	Logic Output B
7	2	7	OUTA	Logic Output A
8	8	8	VDD2	Power Supply for Isolator Side 2

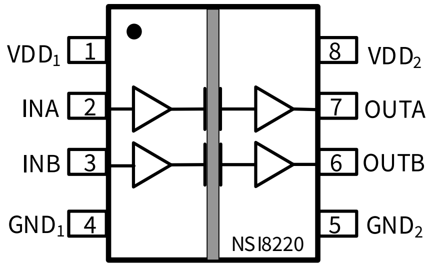


Figure 1.4 NSI8220Cx SOW8 Package

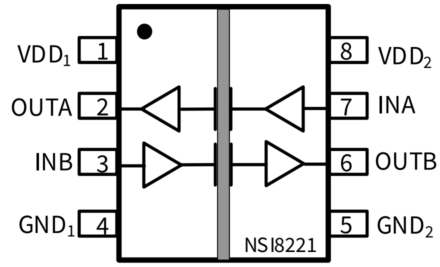


Figure 1.5 NSI8221Cx SOW8 Package

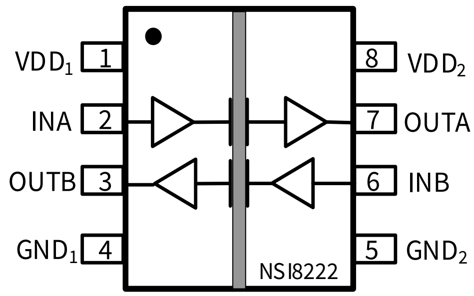


Figure 1.6 NSI8222Cx SOW8 Package

Table1.2 NSI8220C/ NSI8221C/ NSI8222C SOW8 Pin Configuration and Description

NSI8220C PIN NO.	***NSI8221C PIN NO.***	***NSI8222C PIN NO.***	***SYMBOL***	***FUNCTION***
1	1	1	VDD1	Power Supply for Isolator Side 1
2	7	2	INA	Logic Input A
3	3	6	INB	Logic Input B
4	4	4	GND1	Ground 1, the ground reference for Isolator Side 1
5	5	5	GND2	Ground 2, the ground reference for Isolator Side 2
6	6	3	OUTB	Logic Output B
7	2	7	OUTA	Logic Output A
8	8	8	VDD2	Power Supply for Isolator Side 2

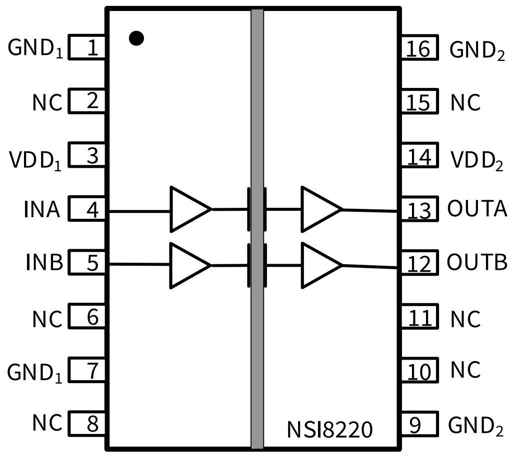


Figure 1.7 NSI8220Cx SOW16 Package

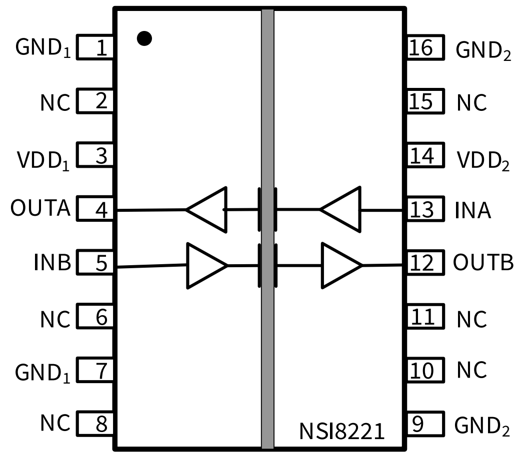


Figure 1.8 NSI8221Cx SOW16 Package

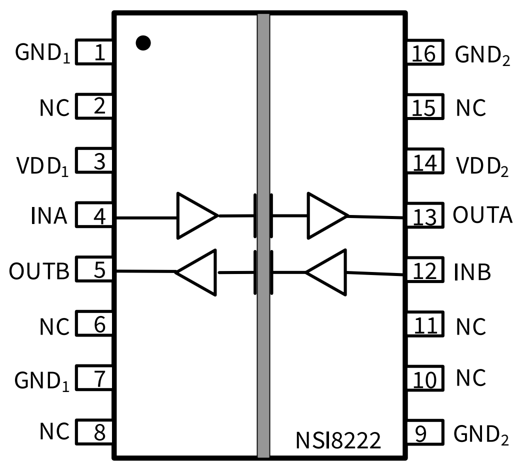


Figure 1.9 NSI8222Cx SOW16 Package

Table 1.3 NSI8220C/ NSI8221C/ NSI8222C SOW16 Pin Configuration and Description

NSI8220C PIN NO.	*NSI8221C PIN NO.*	*NSI8222C PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	1	GND1	Ground 1, the ground reference for Isolator Side 1
2	2	2	NC	No Connection.
3	3	3	VDD1	Power Supply for Isolator Side 1
4	13	4	INA	Logic Input A
5	5	12	INB	Logic Input B
6	6	6	NC	No Connection.

NSI8220C PIN NO.	NSI8221C PIN NO.	NSI8222C PIN NO.	SYMBOL	FUNCTION
7	7	7	GND1	Ground 1, the ground reference for Isolator Side 1
8	8	8	NC	No Connection.
9	9	9	GND2	Ground 2, the ground reference for Isolator Side 2
10	10	10	NC	No Connection.
11	11	11	NC	No Connection.
12	12	5	OUTB	Logic Output A
13	4	13	OUTA	Logic Output B
14	14	14	VDD2	Power Supply for Isolator Side 2
15	15	15	NC	No Connection.
16	16	16	GND2	Ground 2, the ground reference for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	V_{INA}, V_{INB}	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	V_{OUTA}, V_{OUTB}	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	V_{INA}, V_{INB}, V_{OUTA}, V_{OUTB}	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	I_o	-15		15	mA	
Operating Temperature	T_{opr}	-40		125	℃	
Junction Temperature	T_J			150	℃	
Storage Temperature	T_{stg}	-65		150	℃	
Electrostatic discharge	HBM			±8000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	T_{opr}	-40		125	℃
High Level Input Voltage	VIH	2			V
Low Level Input Voltage	VIL			0.8	V
Data rate	DR			150	Mbps

4. Thermal Characteristics

Parameters	*Symbol*	*SOW16*	*SOW8*	*SOP8*	*Unit*
IC Junction-to-Air Thermal Resistance	θ_{JA}	86.5	84.3	137.7	℃/W
Junction-to-case (top) thermal resistance	$\theta_{JC\,(top)}$	49.6	36.3	54.9	℃/W
Junction-to-board thermal resistance	θ_{JB}	49.7	47.0	71.7	℃/W

5. Specifications

5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, T_A =-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, T_A = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power on Reset	VDD_{POR}		2.2		V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
High Level Input Voltage	V_{IH}	2			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Output Voltage	V_{OH}	VDD-0.4			V	$I_{OH} \le 4mA$
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL} \le 4mA$
Output Impedance	R_{out}		50		ohm	
Input Pull high or low Current	I_{pull}		8	15	uA	
Start Up Time after POR	t_{rbs}		10		usec	
Common Mode Transient Immunity	CMTI	±200	±250		kV/us	See Figure 5.8

5.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, T_A =-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** T_A = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSI8220**					
	I_{DD1}(Q0)		0.59	0.89	mA	All Input 0V for NSI8220x0 Or All Input at supply for NSI8220x1
	I_{DD2}(Q0)		1.29	1.94	mA	
	I_{DD1}(Q1)		2.80	4.20	mA	All Input at supply for NSI8220x0 Or All Input 0V for NSI8220x1
	I_{DD2}(Q1)		1.32	1.98	mA	
	I_{DD1}(1M)		1.70	2.55	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.39	2.09	mA	
	I_{DD1}(10M)		1.78	2.67	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.13	3.20	mA	
	I_{DD1}(100M)		2.49	4.23	mA	All Input with 100Mbps, C_L=15pF
	I_{DD2}(100M)		9.22	15.66	mA	
	NSI8221/ NSI8222					
	I_{DD1}(Q0)		0.94	1.41	mA	All Input 0V for NSI822xx0 Or All Input at supply for NSI822xx1
	I_{DD2}(Q0)		0.94	1.41	mA	
	I_{DD1}(Q1)		2.06	3.09	mA	All Input at supply for NSI822xx0 Or All Input 0V for NSI822xx1
	I_{DD2}(Q1)		2.06	3.09	mA	
	I_{DD1}(1M)		1.55	2.32	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.55	2.32	mA	
	I_{DD1}(10M)		1.96	2.93	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		1.96	2.93	mA	
	I_{DD1}(100M)		5.86	10.05	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		5.86	10.05	mA	

5.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, T_A =-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V,** T_A = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSI8220**					
	I_{DD1}(Q0)		0.56	0.83	mA	All Input 0V for NSI8220x0 Or All Input at supply for NSI8220x1
	I_{DD2}(Q0)		1.24	1.86	mA	
	I_{DD1}(Q1)		2.76	4.13	mA	All Input at supply for NSI8220x0 Or All Input 0V for NSI8220x1
	I_{DD2}(Q1)		1.27	1.91	mA	
	I_{DD1}(1M)		1.66	2.49	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.31	1.97	mA	
	I_{DD1}(10M)		1.71	2.57	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		1.80	2.70	mA	
	I_{DD1}(100M)		2.20	3.65	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		6.50	10.77	mA	
	NSI8221/ NSI8222					
	I_{DD1}(Q0)		0.90	1.35	mA	All Input 0V for NSI822xx0 Or All Input at supply for NSI822xx1
	I_{DD2}(Q0)		0.90	1.35	mA	
	I_{DD1}(Q1)		2.01	3.02	mA	All Input at supply for NSI822xx0 Or All Input 0V for NSI822xx1
	I_{DD2}(Q1)		2.01	3.02	mA	
	I_{DD1}(1M)		1.49	2.23	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.49	2.23	mA	
	I_{DD1}(10M)		1.76	2.63	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		1.76	2.63	mA	
	I_{DD1}(100M)		4.35	7.27	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		4.35	7.27	mA	

5.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, T_A =-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V,** T_A = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSI8220**					
	I_{DD1}(Q0)		0.54	0.81	mA	All Input 0V for NSI8220x0 Or All Input at supply for NSI8220x1
	I_{DD2}(Q0)		1.22	1.83	mA	
	I_{DD1}(Q1)		2.73	4.10	mA	All Input at supply for NSI8220x0 Or All Input 0V for NSI8220x1
	I_{DD2}(Q1)		1.24	1.86	mA	
	I_{DD1}(1M)		1.64	2.46	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.27	1.91	mA	
	I_{DD1}(10M)		1.67	2.51	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		1.65	2.48	mA	
	I_{DD1}(100M)		1.98	3.23	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		5.22	8.53	mA	
	NSI8221/ NSI8222					
	I_{DD1}(Q0)		0.88	1.32	mA	All Input 0V for NSI822xx0 Or All Input at supply for NSI822xx1
	I_{DD2}(Q0)		0.88	1.32	mA	
	I_{DD1}(Q1)		1.99	2.98	mA	All Input at supply for NSI822xx0 Or All Input 0V for NSI822xx1
	I_{DD2}(Q1)		1.99	2.98	mA	
	I_{DD1}(1M)		1.46	2.18	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.46	2.18	mA	
	I_{DD1}(10M)		1.66	2.49	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		1.66	2.49	mA	
	I_{DD1}(100M)		3.60	5.93	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		3.60	5.93	mA	

5.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, T_A =-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** T_A = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	6.54	15	ns	See Figure 5.7 , C_L = 15pF
	t_{PHL}	2.5	8.30	15	ns	See Figure 5.7 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.7 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.7 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

5.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, T_A =-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V,** T_A = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	8.0	15	ns	See Figure 5.7 , C_L = 15pF
	t_{PHL}	2.5	8.7	15	ns	See Figure 5.7 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.7 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.7 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

5.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, T_A=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V,** T_A = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	9.0	15	ns	See Figure 5.7 , C_L = 15pF
	t_{PHL}	2.5	9.3	15	ns	See Figure 5.7 , C_L = 15pF
Pulse Width Distortion $\|t_{PHL} - t_{PLH}\|$	PWD			5.0	ns	See Figure 5.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.7, C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.7, C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

5.8. Typical Performance Characteristics

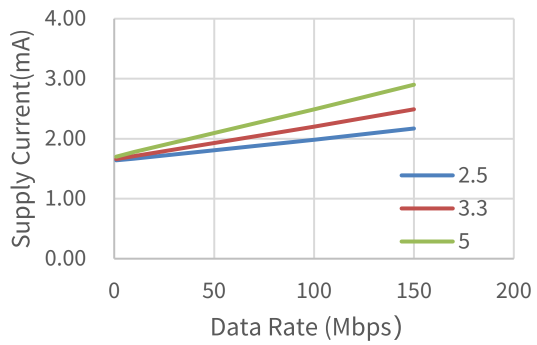


Figure 5.1 NSI8220 VDD1 Supply Current vs Data Rate

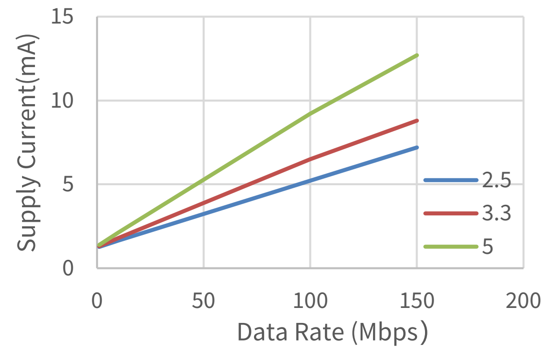


Figure 5.2 NSI8220 VDD2 Supply Current vs Data Rate

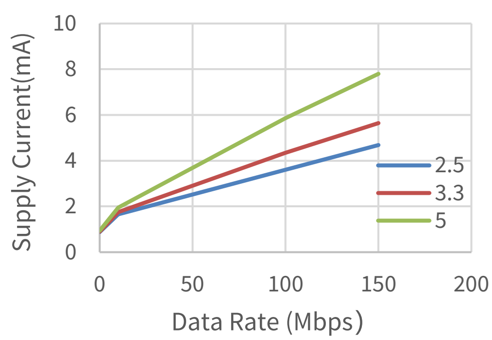


Figure 5.3 NSI8221/ NSI8222 VDD1 Supply Current vs Data Rate

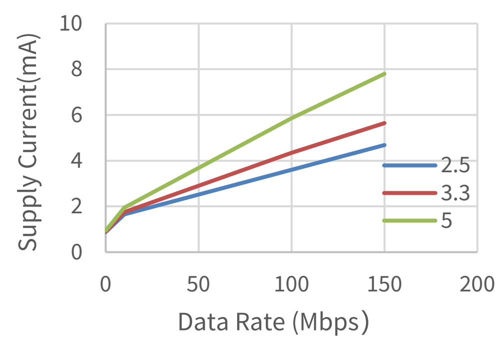


Figure 5.4 NSI8221/ NSI8222 VDD2 Supply Current vs Data Rate

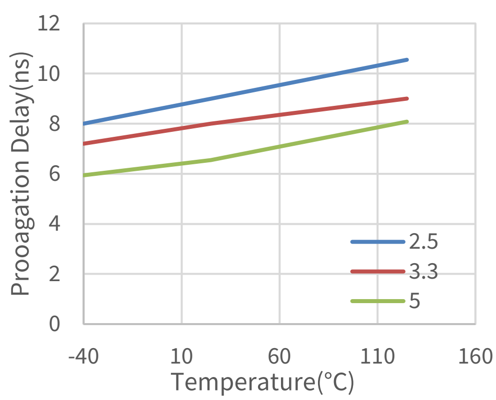


Figure 5.5 Rising Edge Propagation Delay Vs Temp

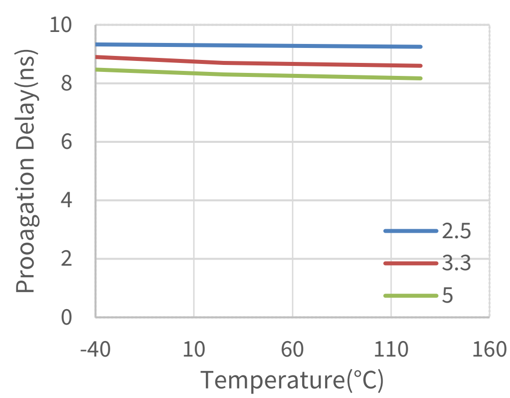


Figure 5.6 Falling Edge Propagation Delay Vs Temp

5.9. Parameter Measurement Information

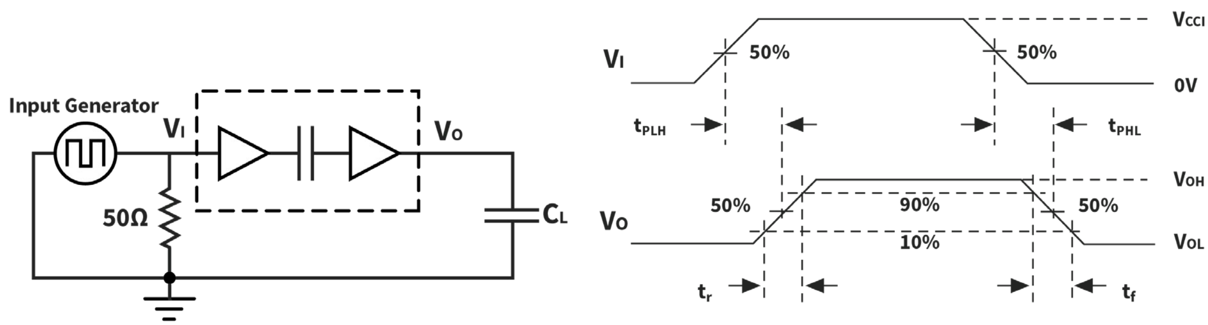


Figure 5.7 Switching Characteristics Test Circuit and Waveform

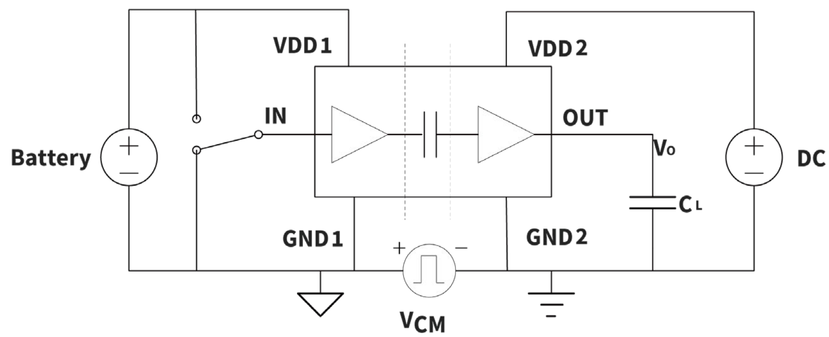


Figure 5.8 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value			Unit	Comments
		SOP8	SOW8	SOW16		
Minimum External Clearance	CLR	4.0	8.0	8.0	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	4.0	8.0	8.0	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28			um	
Tracking Resistance (Comparative Tracking Index)	CTI	>600	>600	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I	I	I		IEC 60664-1

Description	Test Condition	Value		
		SOP8	SOW8	SOW16
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV	I to IV	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to III	I to IV	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to II	I to IV	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I	I to III	I to III
Climatic Classification		40/125/21		
Pollution Degree per DIN VDE 0110,		2		

6.2. Insulation Characteristics

Description	Test Condition	Symbol	Value			Unit
			SOP8	SOW8	SOW16	
Maximum repetitive isolation voltage		V_{IORM}	565	2121	2121	V_{PEAK}
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	400	1500	1500	V_{RMS}
	DC voltage		565	2121	2121	V_{DC}

Description	Test Condition	Symbol	Value SOP8	Value SOW8	Value SOW16	Unit
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.					pC
Apparent Charge	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s	q_{pd}		<5	<5	pC
Apparent Charge	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.875*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)					pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.					pC
Apparent Charge	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.3*V_{IORM}, t_m=10s	q_{pd}	<5			pC
Apparent Charge	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.5*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)					pC
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	5300	8000	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	5384	6250	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{IOSM} \geqslant V_{IMP} \times 1.3$	V_{IOSM}	7000	10000	10000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25℃	R_{IO}	>10^{12}	>10^{12}	>10^{12}	Ω

Description	Test Condition	Symbol	Value			Unit
			SOP8	SOW8	SOW16	
	V_{IO} =500V, 100℃ ≤ T_{amb} ≤ 125℃		>10^{11}	>10^{11}	>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_s		>10^9	>10^9	>10^9	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.6	0.6	0.6	pF
UL1577						
Withstand Isolation Voltage	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production test)	V_{ISO}	3750	5000	5000	V_{RMS}

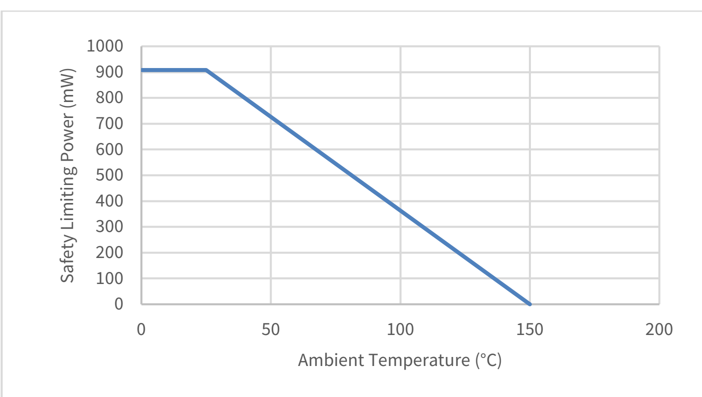
6.3. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE 0884-17 of NSI822xC-DSPR SOP8(150mil)

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{θJA}$ = 137.7 ℃/W, T_J = 150 ℃, T_A = 25 ℃	908	mW
Safety Supply Current	$R_{θJA}$ = 137.7 ℃/W, V_I = 5.5 V, T_J = 150 ℃, T_A = 25 ℃	165	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{θJA}$, of SOP8(150mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.



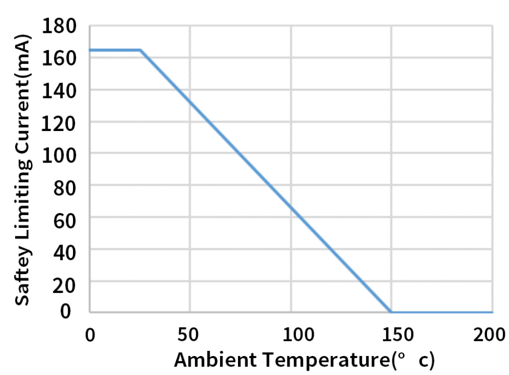


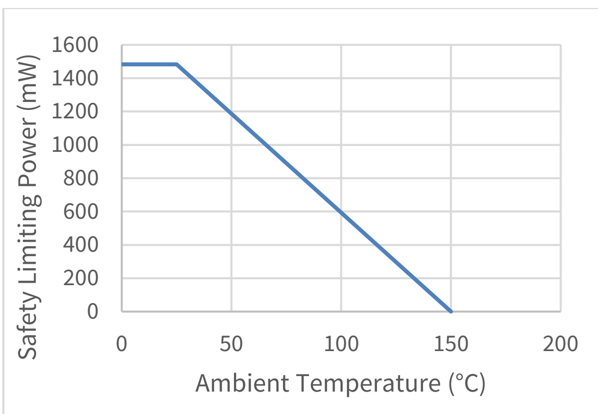
Figure 6.1 NSI822xC-DSPR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI822xC-DSWVR SOW8(300mil)

Description	***Test Condition***	***Value***	***Unit***
Safety Supply Power	$R_{θJA}$ = 84.3 ℃/W, V_I = 5.5 V, T_J = 150 ℃, T_A = 25 ℃	1483	mW
Safety Supply Current	$R_{θJA}$ = 84.3 ℃/W, T_J = 150 ℃, T_A = 25 ℃	269.6	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{θJA}$, of SOW8(300mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.



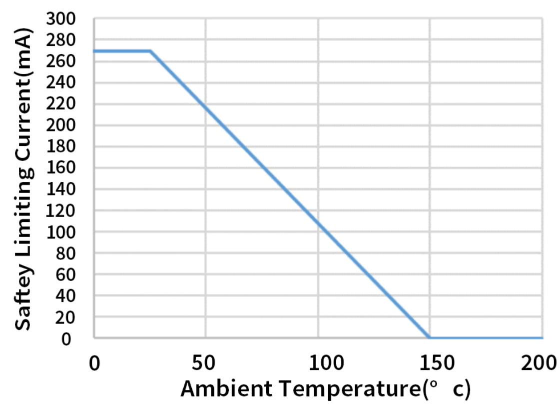


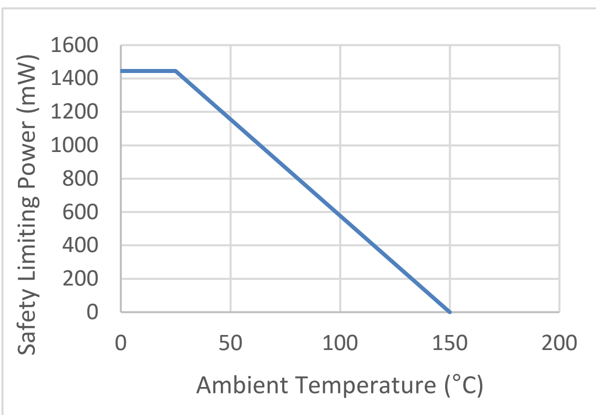
Figure 6.2 NSI822xC-DSWVR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

Reinforced isolation safety-limiting values as outlined in VDE 0884-17 of NSI822xC-DSWR SOW16(300mil)

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA}$ = 86.5 ℃/W, V_I = 5.5 V, T_J = 150 ℃, T_A = 25 ℃	1445	mW
Safety Supply Current	$R_{\theta JA}$ = 86.5 ℃/W, T_J = 150 ℃, T_A = 25 ℃	262.7	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOW16(300mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.



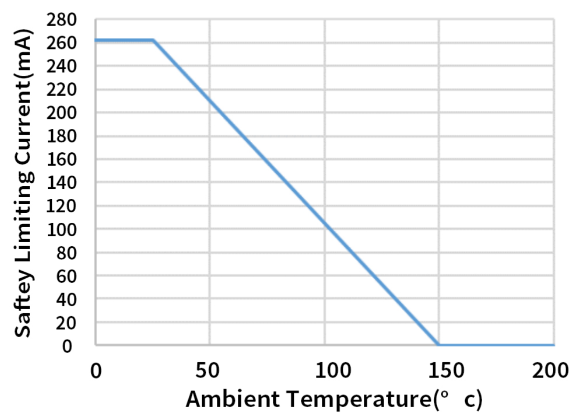


Figure 6.3 NSI822xC-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

6.4. Regulatory Information

The NSI822xC-DSPR are approved by the organizations listed in table.

CUL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022	Certified According to EN IEC 62368-1
Single Protection, 3750V_{rms} Isolation voltage	Single Protection, 3750V_{rms} Isolation voltage	Basic Insulation V_{IORM}=565Vpeak V_{IOTM}=5300Vpeak V_{IOSM}=7000Vpeak	Basic insulation	3000Vrms for 1min
File (E500602)	File (E500602)	File (40050121)	File (CQC20001264940)	R50574061

The NSI822xC-DSWVR are approved by the organizations listed in table.

CUL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022	Certified According to EN IEC 62368-1
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforced Insulation V_{IORM}=2121Vpeak V_{IOTM}=8000Vpeak V_{IOSM}=10000Vpeak	Reinforced insulation	5000Vrms for 1min
File (E500602)	File (E500602)	File (40052820)	File (CQC20001264938)	R50574061

The NSI822xC-DSWR are approved by the organizations listed in table.

CUL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022	Certified According to EN IEC 62368-1
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforced Insulation V_{IORM}=2121Vpeak V_{IOTM}=8000Vpeak V_{IOSM}=10000Vpeak	Reinforced insulation	5000Vrms for 1min
File (E500602)	File (E500602)	File (40052820)	File (CQC20001264939)	R50574061

7. Function Description

7.1. Overview

The NSI822x is a Dual-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSI822x device is safety certified by UL1577 support several insulation withstand voltages (3.75kV_{rms}, 5kV_{rms}), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI822x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/us. The NSI822x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI822x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSI822x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 7.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 60us after powering up.

Table 7.1 Output status vs. power status

<table>
<tr><th>Input[1]</th><th>VDDIN status</th><th>VDDOUT status</th><th>Output</th><th>Comment</th></tr>
<tr><td>H</td><td>Ready</td><td>Ready</td><td>H</td><td rowspan="2">Normal operation.</td></tr>
<tr><td>L</td><td>Ready</td><td>Ready</td><td>L</td></tr>
<tr><td>X</td><td>Unready</td><td>Ready</td><td>L(NSI822xx0)
H(NSI822xx1)</td><td>The output follows the same status with the input within 60us after input side VDD is powered on.</td></tr>
<tr><td>X</td><td>Ready</td><td>Unready</td><td>Undetermined</td><td>The output follows the same status with the input within 60us after output side VDD is powered on.</td></tr>
<tr><td colspan="5">Note: H=Logic high; L=Logic low; X=Logic low or logic high
VDDIN is input side power; VDDOUT is output side power.
(1) There is a protection diode between the input and the VDDIN. When the VDDIN is floating, the strong drive signal through the input pin will put the VDDIN in an indeterminate state.</td></tr>
</table>

7.2. OOK Modulation

NSI822x is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 7.1, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

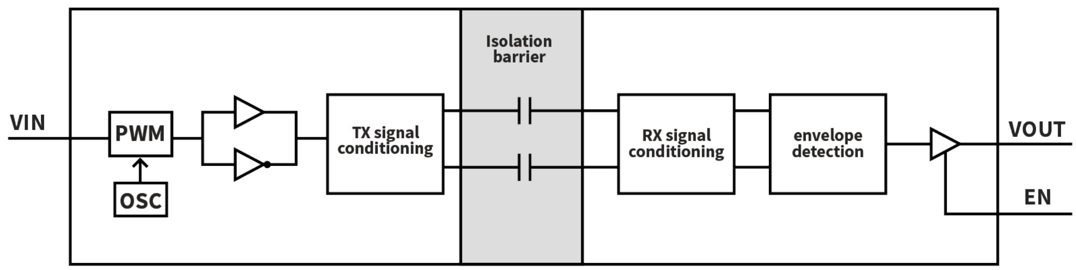


Figure 7.1 Single Channel Function Block Diagram

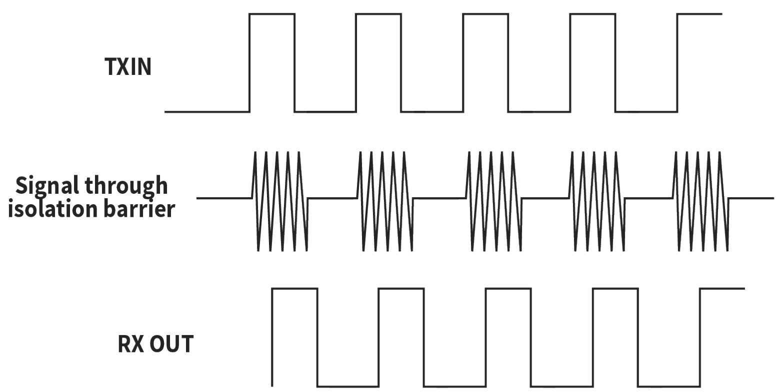


Figure 7.2 OOK Modulation

8. Application Note

8.1. Typical Application Circuit

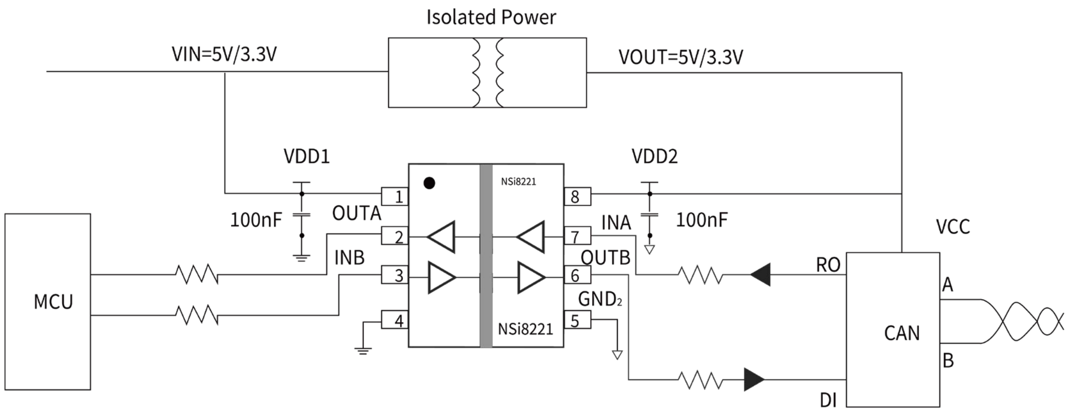


Figure 8.1 Typical SCH for ISO CAN Interface

8.2. PCB Layout

The NSI822x requires a 0.1 µF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be

placed as close as possible to the package. Figure 8.2 to Figure 8.5 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

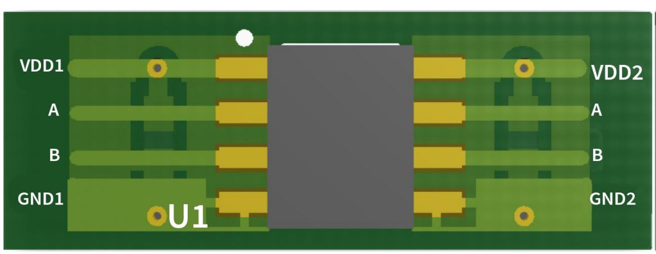


Figure8.2 Recommended PCB Layout — Top Layer

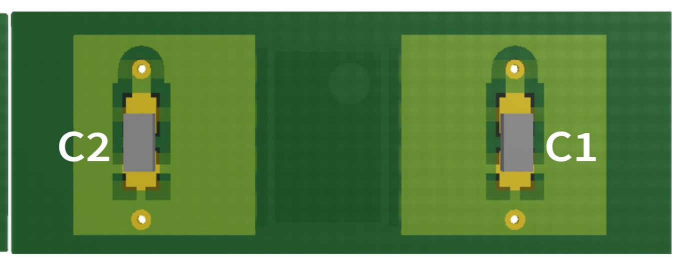


Figure8.3 Recommended PCB Layout — Bottom Layer

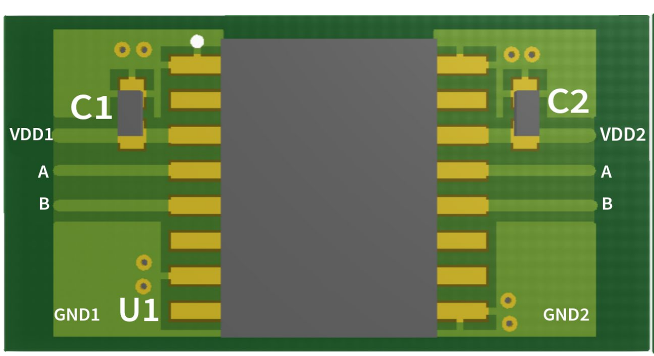


Figure8.4 Recommended PCB Layout — Top Layer

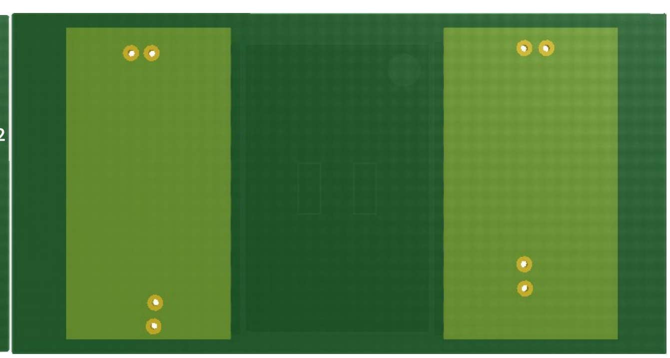


Figure8.5 Recommended PCB Layout — Bottom Layer

8.3. High Speed Performance

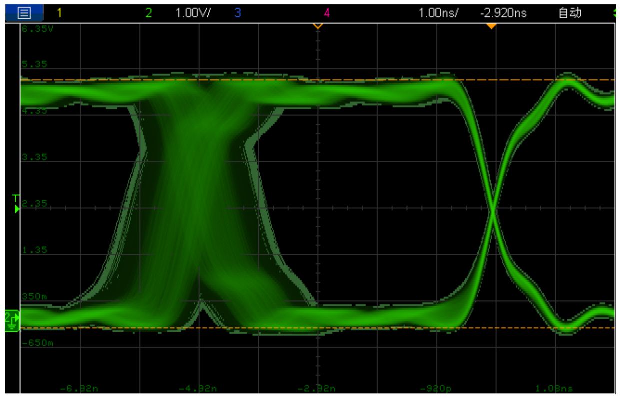


Figure8.6 Eye Diagram

8.4. Typical Supply Current Equations

The typical supply current of NSI822x can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF

NSI8220:

$I_{DD1} = 0.19 * a1 + 1.45 * b1 + 0.82 * c1.$

$I_{DD2} = 1.36 + VDD2 * f * C_L * c1 * 10^{-9}$

When a1 is the channel number of default state input at side 1, b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1.

NSI8221/ NSI8222:

$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$

$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD2 * f * C_L * c1 * 10^{-9}$

When b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1, b2 is the channel number of non-default state input at side 2, c2 is the channel number of switch signal input at side 2.

9. Package Information

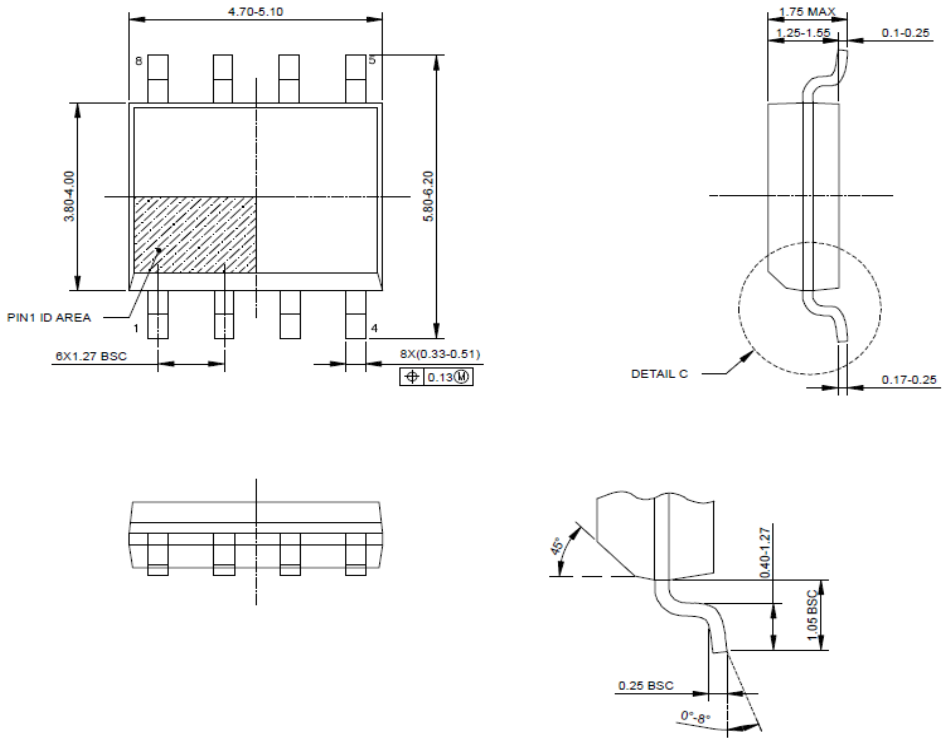
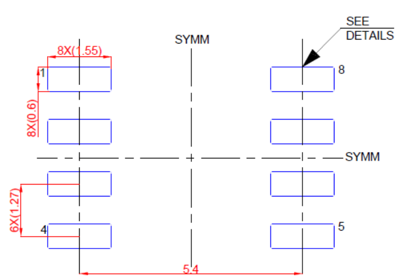
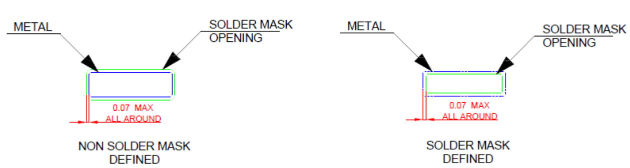


Figure 9.1 SOP8 Package Shape and Dimension in millimeters

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

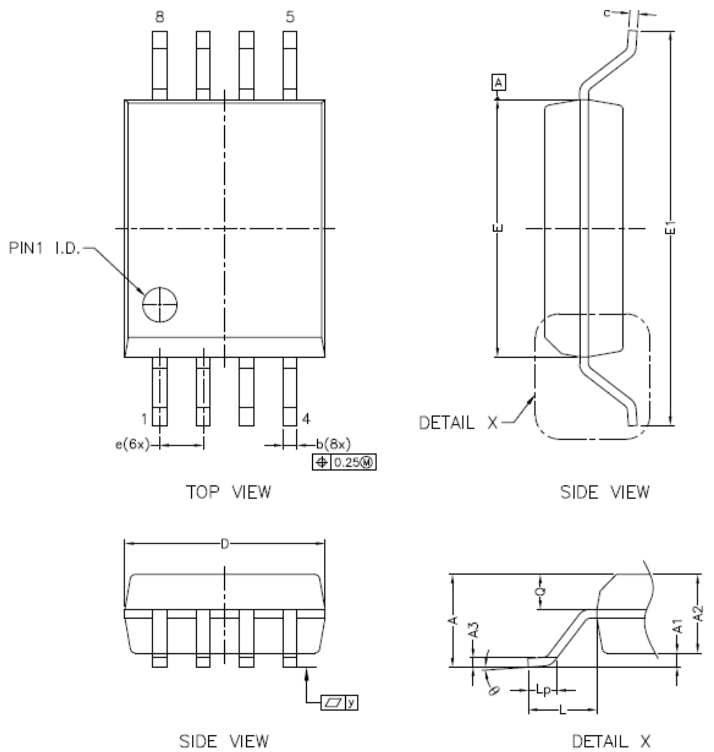


LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 9.2 SOP8 Package Board Layout Example



* CONTROLLING DIMENSION : MM

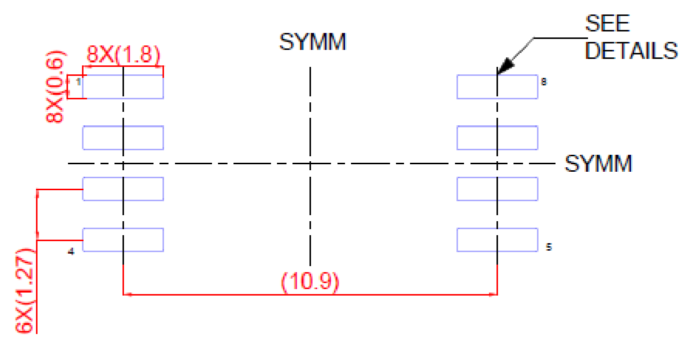
SYMBOL	MM MIN.	MM NOM.	MM MAX.
A	--	--	2.80
A1	0.36	--	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	--	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	--	1.00
y	--	0.10	--
θ	0°	--	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 9.3 SOW8 Package Shape and Dimension in millimeters

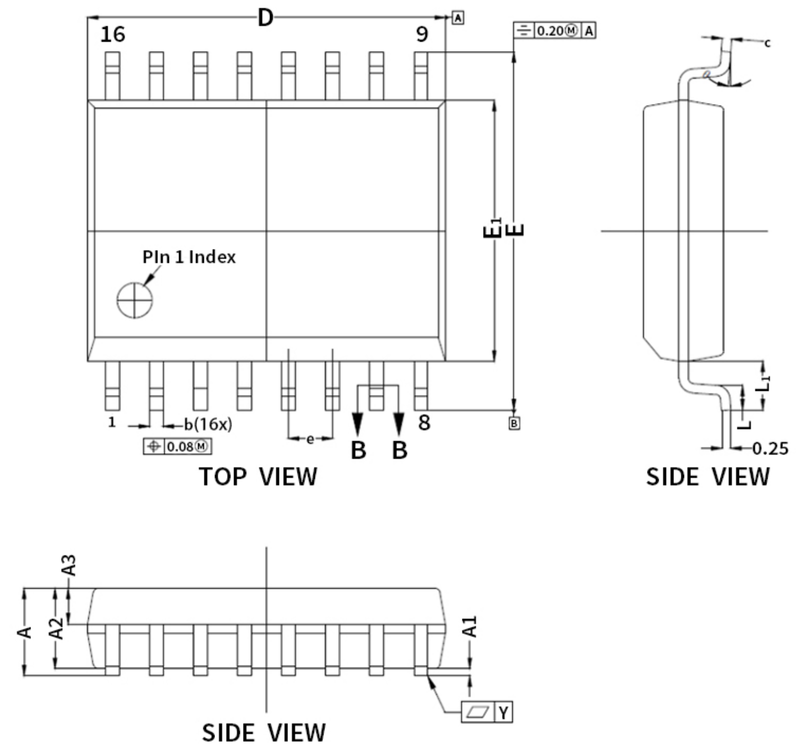
NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.



LAND PATTERN EXAMPLE(mm)
9.1 mm NOMINAL
CLEARANCE/CREEPAGE

SOLDER MASK DETAILS

Figure 9.4 SOW8 Package Board Layout Example



* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0^{0}	---	8^{0}

NOTES
1.0 COPWNARITY APPUES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 9.5 SOW16 Package Shape and Dimension in millimeters

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

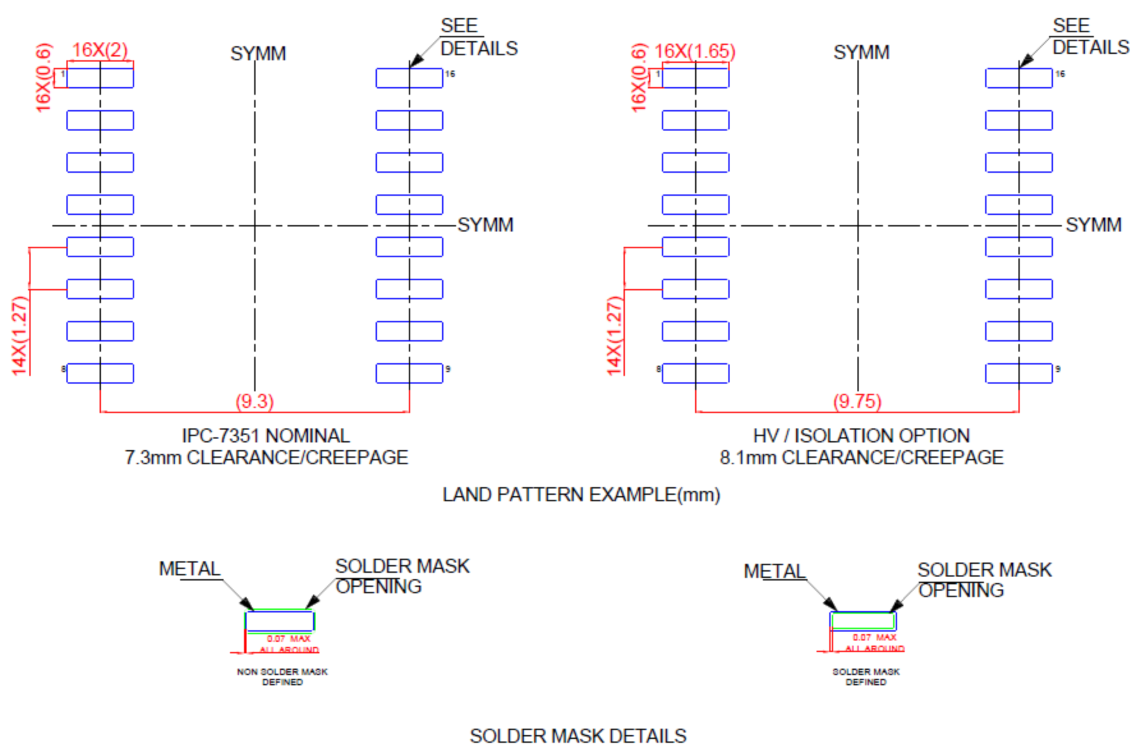


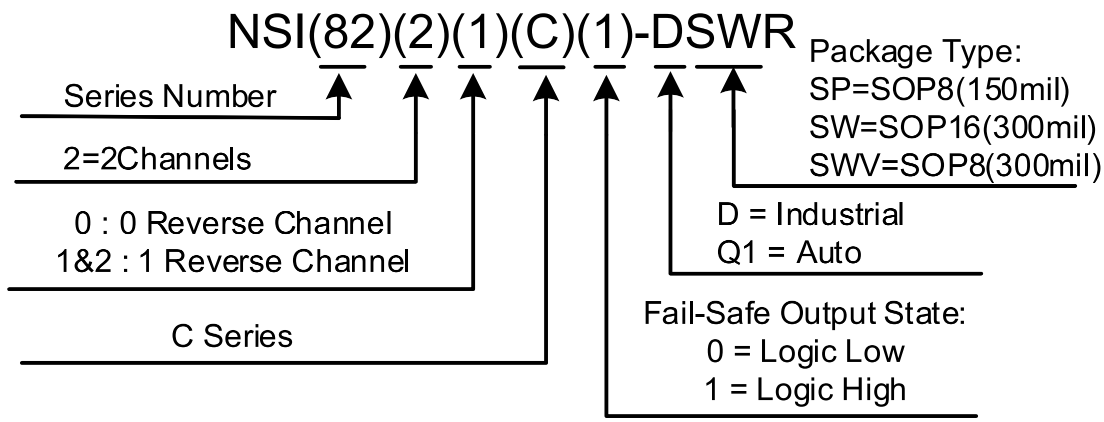
Figure 9.6 SOW16 Package Board Layout Example

10. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSI8220C0-DSPR	3.75	2	0	150	Low	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8220C1-DSPR	3.75	2	0	150	High	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8221C0-DSPR	3.75	1	1	150	Low	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8221C1-DSPR	3.75	1	1	150	High	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8222C0-DSPR	3.75	1	1	150	Low	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8222C1-DSPR	3.75	1	1	150	High	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8220C0-DSWR	5	2	0	150	Low	-40 to 125℃	3	SOW16 (300mil)	SOW16	1000
NSI8220C1-DSWR	5	2	0	150	High	-40 to 125℃	3	SOW16 (300mil)	SOW16	1000
NSI8221C0-DSWR	5	1	1	150	Low	-40 to 125℃	3	SOW16 (300mil)	SOW16	1000
NSI8221C1-DSWR	5	1	1	150	High	-40 to 125℃	3	SOW16 (300mil)	SOW16	1000
NSI8222C0-DSWR	5	1	1	150	Low	-40 to 125℃	3	SOW16 (300mil)	SOW16	1000
NSI8222C1-DSWR	5	1	1	150	High	-40 to 125℃	3	SOW16 (300mil)	SOW16	1000
NSI8220C0-DSWVR	5	2	0	150	Low	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8220C1-DSWVR	5	2	0	150	High	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8221C0-DSWVR	5	1	1	150	Low	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8221C1-DSWVR	5	1	1	150	High	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8222C0-DSWVR	5	1	1	150	Low	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8222C1-DSWVR	5	1	1	150	High	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 ℃ according to the JEDEC industry standard classifications and peak solder temperatures.

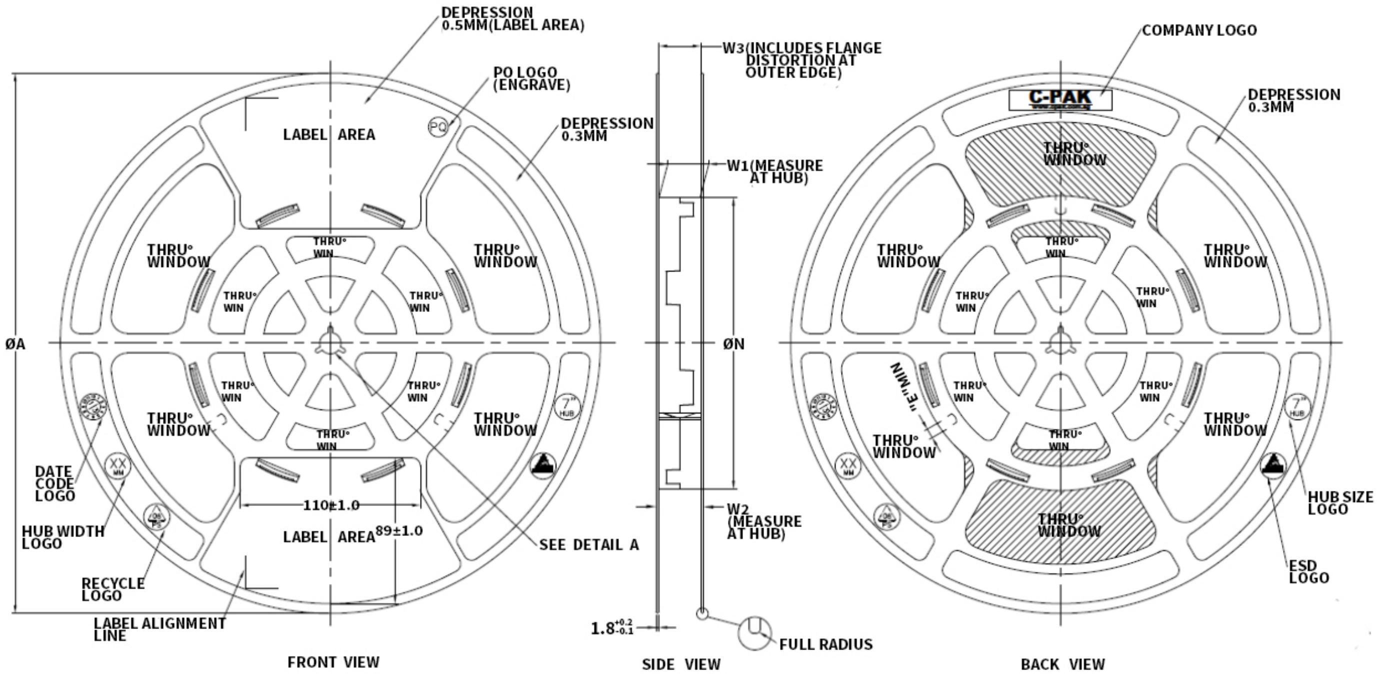
Part Number Rule:

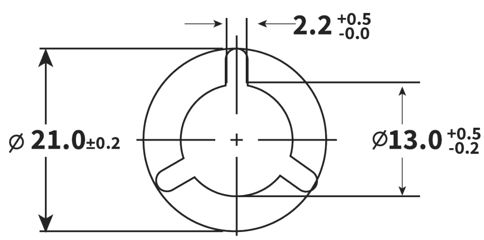


11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSI822xC	tbd	tbd	tbd	tbd

12. Tape and Reel Information



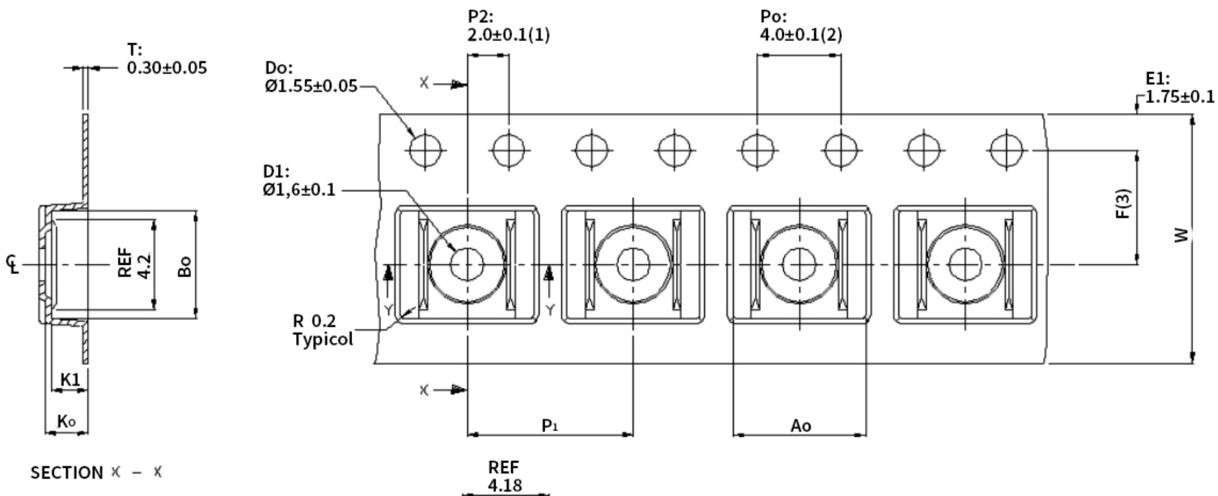


ARBOR HOLE
DETAIL A
SCALE: 3:1

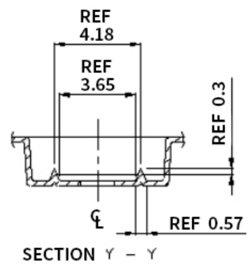
PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

Figure 12.1 Reel Information (for all packages)

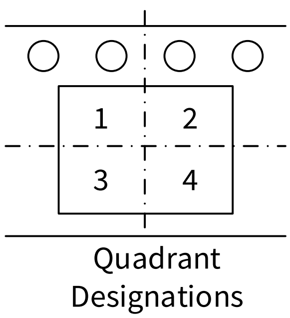


Ao	6.50+/-0.1
Bo	5.30+/-0.1
Ko	2.20+/-0.1
K1	1.90+/-0.1
F	5.50+/-0.1
P1	8.00+/-0.1
W	12.00+/-0.3



(1) Measured from centrellne of sprocket hole to centreline of pocket
(2) cumulotive tolerance of 10 sprocket holes is ±0.20
(3) Measured from centrellne of sprocket hole to centreline of pocket
(4) Other material ovoilable

ALL DIMENSIONS IN MILLIME TRES UNLESS OTHERWISE STATED



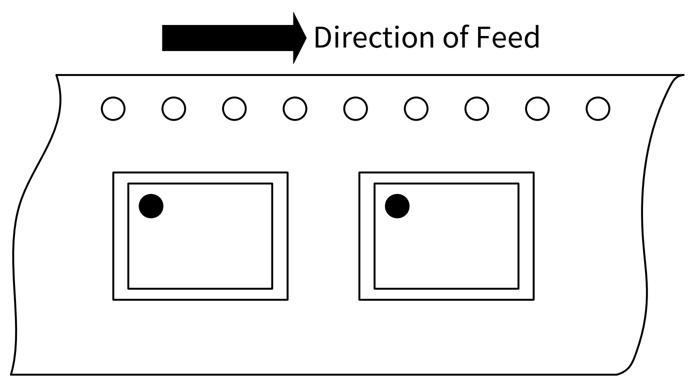
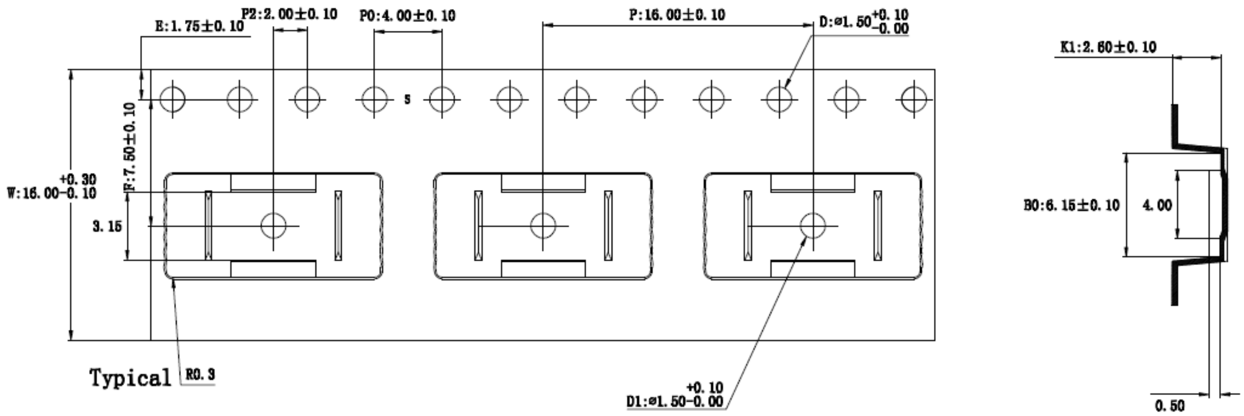
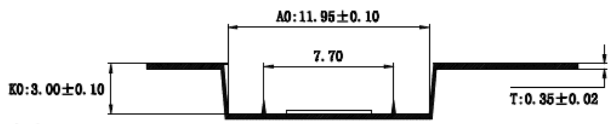


Figure 12.2 Tape Information of SOP8



技术要求:
Technical Requirements:



1. 每10个料带链孔径累计公差为±0.20毫米。
   10 sprocket hole pitch cumulative toleran±0.20mm
2. 料带弯曲每250毫米不可超过1毫米。
   Carrier camber is within 1 mm in 250 mm
3. 所有尺寸符合EIA-481-D标准要求。
   All dimensions meet EIA-481-D requirements

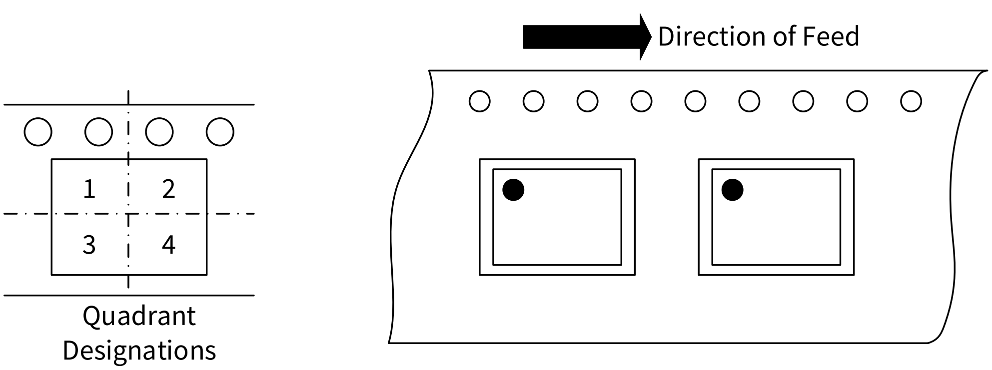
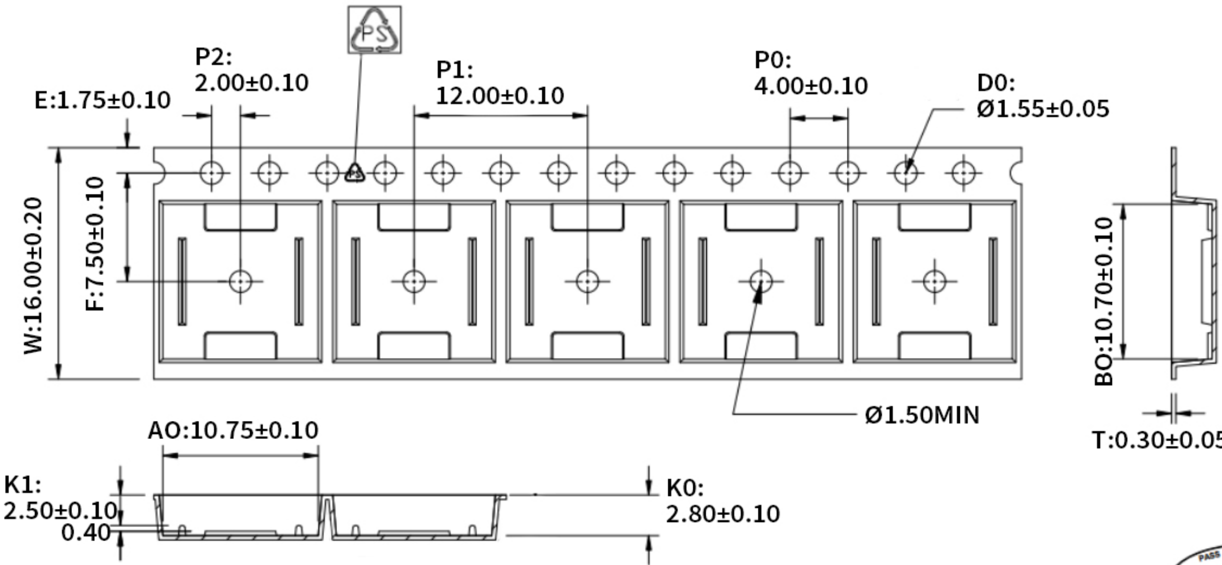
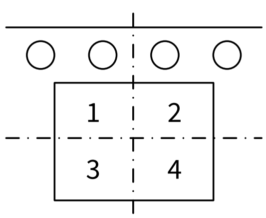


Figure 12.3 Tape Information of SOW8



1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30±0.05mm.
6. Packing length per 22" reel: 378 Meters.(Rewind N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity: 10^5~ 10^{10}Ω/□

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10



Quadrant Designations

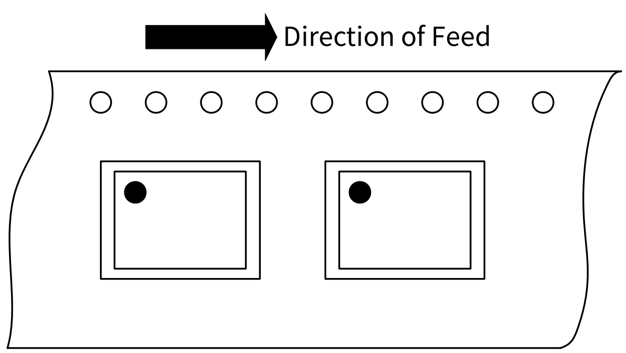


Figure 12.4 Tape Information of SOW16

13. Revision History

Revision	Description	Date
1.0	Initial version	2021/9/20
1.1	Update Insulation and Safety Related Specifications, add Thermal Derating Curve, add Junction Temperature, delate "Isolation barrier life: >60 years", delate AEC-Q100， update Regulatory Information VDE file. Correct MSL.	2022/9/7
1.2	Correct the operating temperature	2023/2/2
1.3	Update Regulatory Information and Safety Regulatory Approvals. Correct Typical Supply Current Equations. Improved the description of $V_{pd(m)}$ in Section 6.1. Change the typical CMTI from 150 to 250 kV/us, change the minimum CMTI from 100 to 200 kV/us, change the maximum Data rate from 100 to 150 Mbps, change the CTI of SOP8 from 400 to 600, change the Material Group of SOP8 from II to I.	2023/5/30
1.4	Remove VIT from electrical parameters to avoid misunderstanding. Correct formatting and images. Update Safety certification info throughout the document. Update Package Information and Tape and Reel Information. Update Function Description.	2024/7/30

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