晶源健三电子

SIC-module driver board-V1.0 碳化硅模块驱动电路板产品说明书

编　制: _____ 日　期: _____

审　核: _____ 日　期: _____

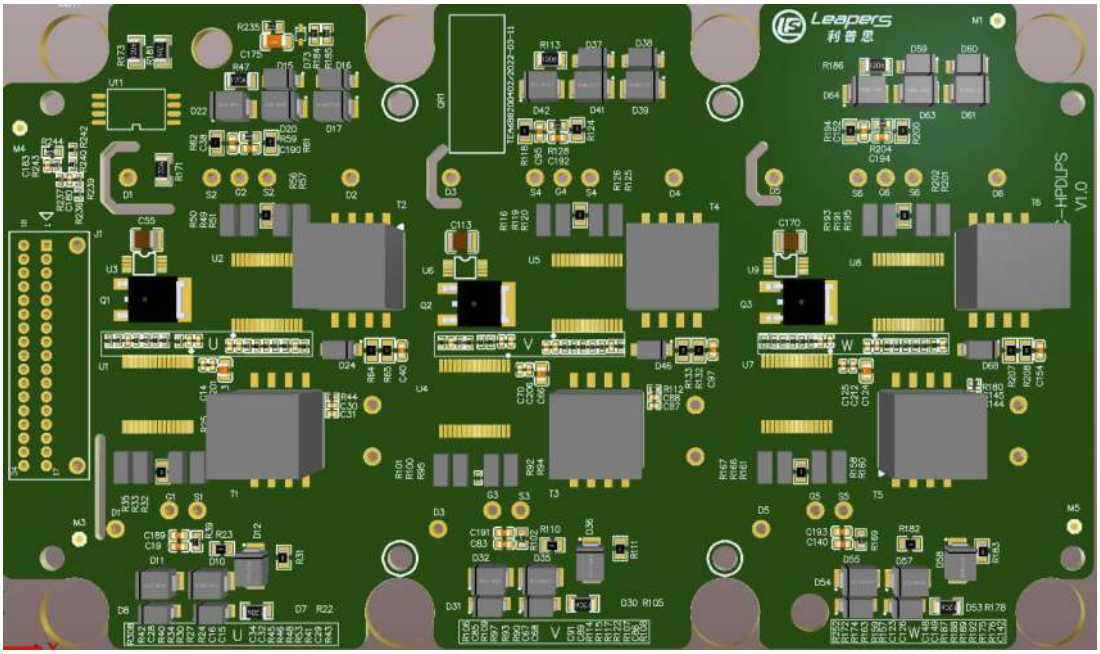
归　档: _____ 日　期: _____

SIC-module driver board-V1.0

Starpower 碳化硅驱动电路板产品说明书

一、产品概述

SIC-module driver board 碳化硅驱动电路板一款针对碳化硅功率半导体模块的智能驱动电路板。该驱动器专门针对斯达的碳化硅功率半导体模块的驱动电路板。该 PCB 板长宽尺寸为 159*94mm。产品正面俯视图如下:



二、产品特点

- 门极最大输出峰值电流 ± 15A
- 快速碳化硅功率半导体模块退饱和检测保护功能，检测时间< 3us
- 过流 OC 及 SC 检测
- 兼容光耦高压 AD 采样及驱动芯片隔离 SPI 通讯两种 V_{DC} 采样功能
- 有源米勒钳位功能
- 有源钳位功能
- 支持两极关断和软关断
- 支持原边、副边供电欠压保护
- 兼容支持高压（驱动芯片隔离 SPI 采样）、低压 NTC 检测，大于 4mm 爬电
- 变压器爬电大于 10mm,电气间隙大于 8mm
- 隔离 SPI 智能数字接口，参数灵活配置，状态监控
- -40℃~ 125° C 宽工作温度范围
- 满足车规级功能安全要求

三、碳化硅功率半导体模块驱动电路板功能框图

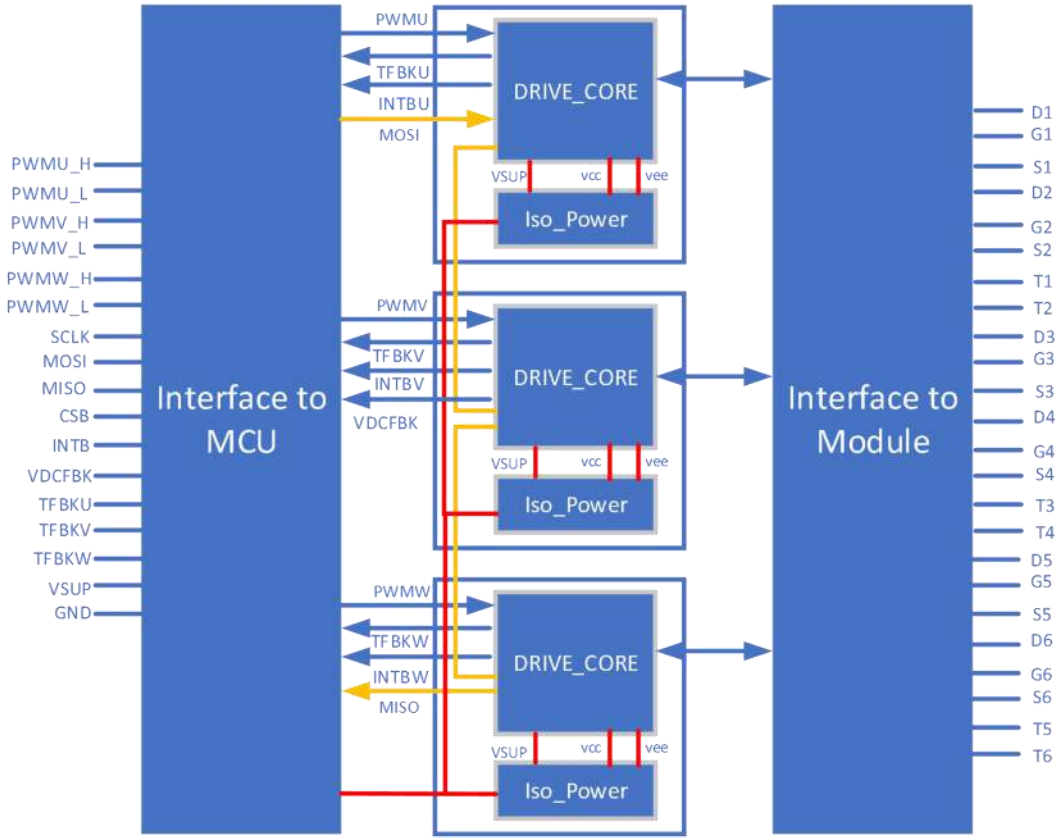
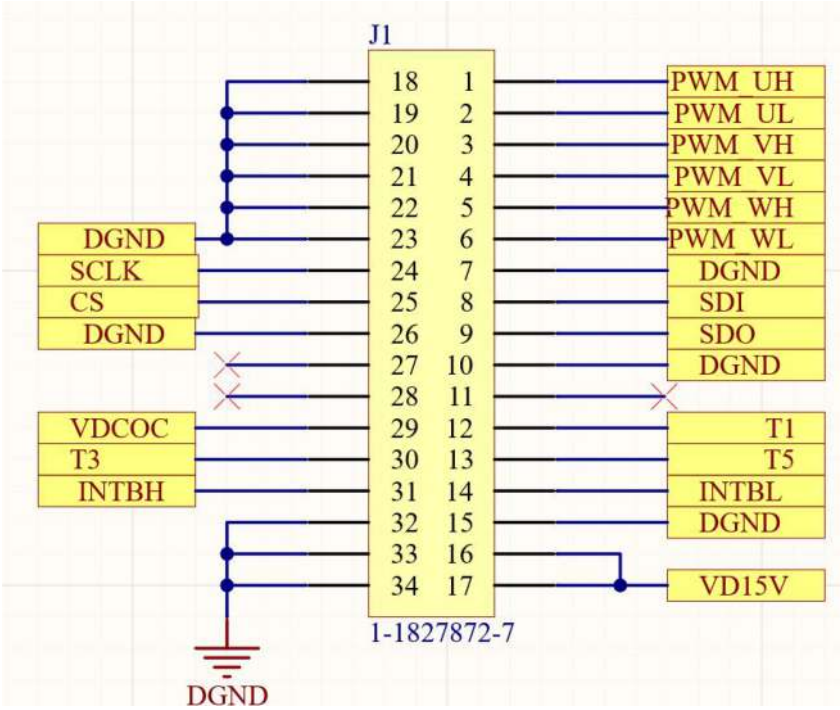


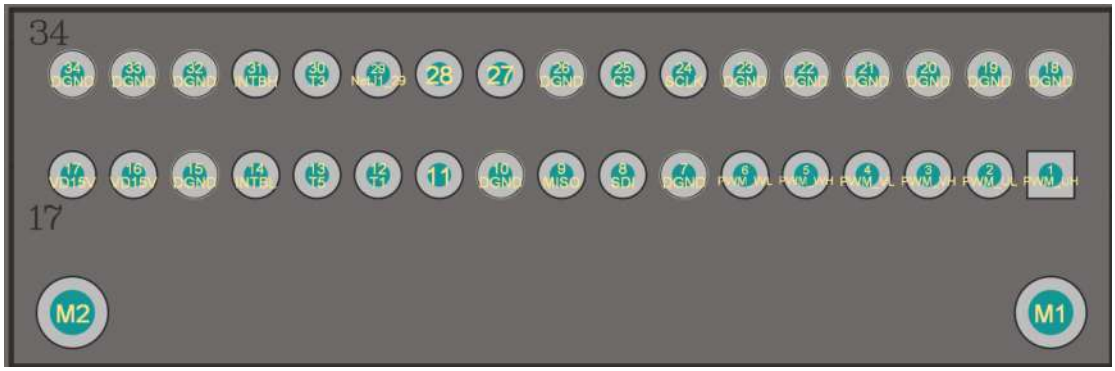
图 2 驱动电路板功能框图

四、接口定义及电气特性

4.1 PCB 接口端子引脚原理图



4.2 连接器接口 PCB 正面俯视图



4.3 端子电气属性说明表

该碳化硅功率半导体模块驱动电路板接插件采用 34PIN 2mm 间距双排插针，管脚定义如下：

描述	名字	PIN	PIN	名字	描述
U 相上管 PWM 输入	PWM_UH	1	18	DGND	控制地
U 相下管 PWM 输入	PWM_UL	2	19	DGND	控制地

V 相上管 PWM 输入	PWM_VH	3	20	DGND	控制地
V 相下管 PWM 输入	PWM_VL	4	21	DGND	控制地
W 相上管 PWM 输入	PWM_WH	5	22	DGND	控制地
W 相下管 PWM 输入	PWM_WL	6	23	DGND	控制地
控制地	DGND	7	24	SCLK	SPI 时钟输入
SPI 从机输入	SDI (MOSI)	8	25	CS	SPI 片选信号输入
SPI 从机输出	SDO (MISO)	9	26	DGND	控制地
控制地	DGND	10	27	-	NC
NC	-	11	28	-	NC
U 相模块温度检测（0~5V）	T1	12	29	VDCOC	母线电压光耦采样
W 相模块温度检测（0~5V）	T5	13	30	T3	V 相模块温度检测（0~5V）
下管故障信号	INTBL	14	31	INTBH	上管故障信号
控制地	GND	15	32	DGND	控制地
控制板供电电源输入	VD15V	16	33	DGND	控制地
控制板供电电源输入	VD15V	17	34	DGND	控制地

4.4 板件电气特性表

如无特殊说明，测试条件为 T = 25 °C, V_{SUP} = 12V

参数	符号	参数说明	最小值	典型值	最大值	单位
输入电源	V_{sup}	驱动电路板供电	8	12	18	V
静态功耗	P_{sd}			5		W
峰值电流	I_{peak}	驱动板输出峰值电流	-15		+15	A
门极开通电压	V_{gsh}	门极正压		15		V
门极关断电压	V_{gsl}	门极负压		-3		V
副边欠压保护	V_{UVLO-}	VCC 对 VE 的电压（可设置）	10	11.5	13.5	V
开通阈值	V_{pwmh}		2.31			V
关断阈值	V_{pwml}				0.99	V
短路保护电流	I_{Desat}	退饱和检测电流（可设置）	250	500	1000	uA
短路保护时间	T_{Desat}				3	uS
短路保护阈值	V_{Desat}	退饱和保护电压阈值（可设置）	3	6	10	V
二级关断电压	V_{2LTO}	二级关断电压（可设置）	8.9	9.96	11.89	V
软关断电流	I_{SSD}	软关断电流（可设置）	0.094	0.541	0.996	A
开通延迟	T_{don}	原边 PWM 到副边门极	75		125	ns
关断延时	T_{doff}	原边 PWM 到副边门极	75		125	ns
PWM 频率	F_{pwm}			20	50	kHz
工作温度	T_A		-40		125	°C

五、输入电源

该碳化硅功率半导体模块驱动电路板推荐输入电源 12V。但支持输入电压 12V-28V. 该碳化硅功率半导体模块驱动电路板把副边输出电压稳定在 18V，门极开通电压 15V，门极关断电压-3V。该碳化硅功率半导体模块驱动电路板内部有 5V 线性稳压器，提供原边 5V 驱动自供电电源及信号上下接电源，但不推荐给其它芯片带载。(具体电压视驱动板型号而定，有 3.3V 版本和 5V 版本，默认为 5V)

六、PWM 信号输入

该碳化硅功率半导体模块驱动电路板提供 6 路 PWM 信号输入，每路 PWM 控制一个碳化硅 MOSFET 开通与关断，6 路 PWM 信号为+5V（默认 5V），低电平 0V 的 PWM 信号。

七、有源钳位

有源钳位可以防止碳化硅功率半导体模块过压损坏，其原理是当 V_{ds} 电压尖峰超过一个预设门槛时，有源钳位电路会启动，使碳化硅 MOSFET 的 V_{ds} 电压得到抑制。
有源钳位电路通过在 D,G 端用瞬态抑制二极管（TVS）来建立反馈通路。
目前，驱动电路板预设的 TVS 管的钳位电压在 1060V 左右。

八、门极电阻

该碳化硅功率半导体模块预设了门极电阻，客户可根据自己的实际应用进行调整。

位号 / 类型		U_H	U_L	V_H	V_L	W_H	W_L
R_{on}	10R	R25,R26,	R49,R50,	R92,R94,	R116,R119,	R158,R160,	R191,R193
R_{off}	10R	R33,R35	R56,R57	R100,R101,	R125,R126,	R166,R167,	R201,R202
c_{gs}	10nF	C189	C190	C191	C192	C193	C194

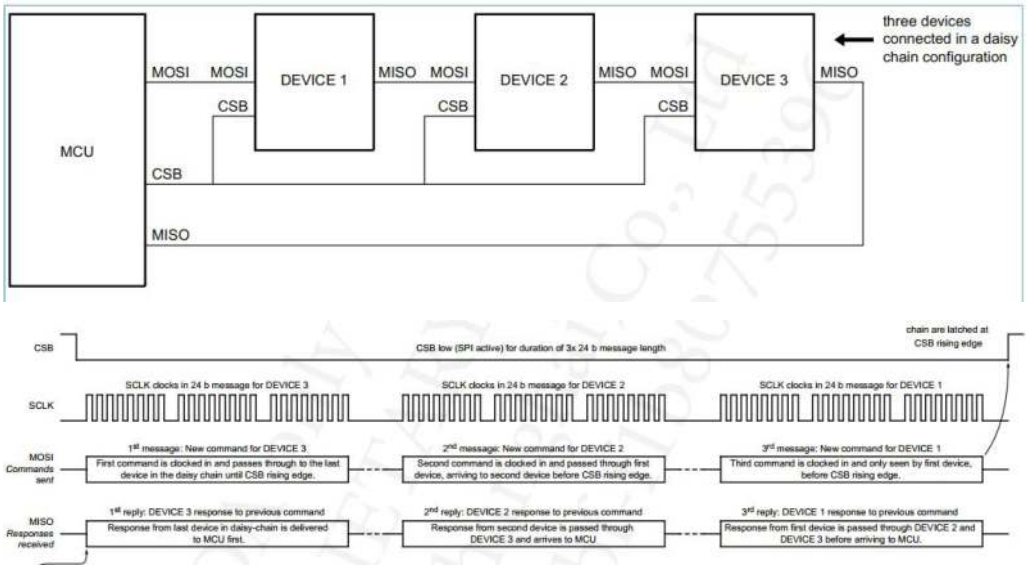
九、SPI 数字接口

该碳化硅功率半导体模块驱动电路板提供 SPI 数字接口，可通过 SPI 数字接口对碳化硅功率半导体模块驱动电路板的一些保护功能和参数进行设置，另外，可通过 SPI 口查询碳化硅功率半导体模块驱动电路板的状态及一些检测反馈值，如 VDC，温度等。推荐 SCLK 频率 500kHz-600kHz。

该碳化硅功率半导体模块驱动电路板有 6 路驱动信号，6 路驱动信号通过菊花链方式连接，

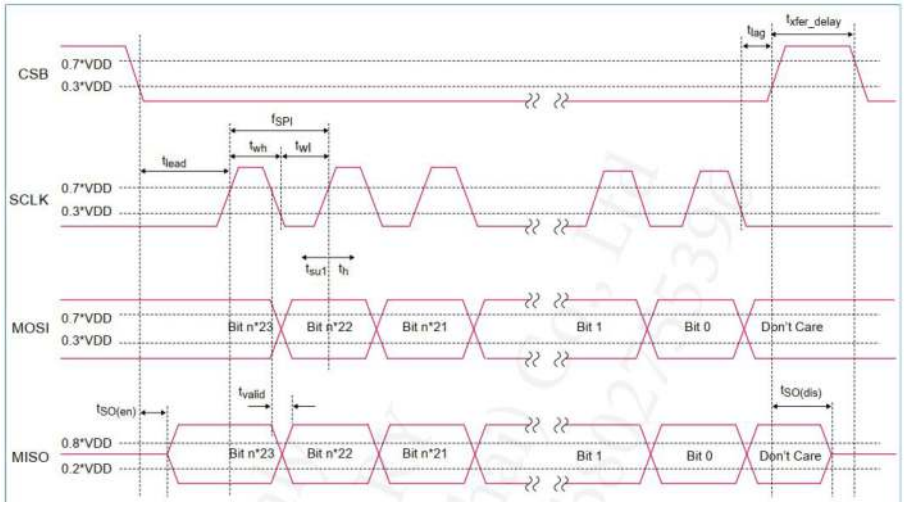
共用一个 SPI 接口，即 SCLK, CSB, SDI（MOSI）, SDO（MISO）。

3 路驱动菊花链相连示例：

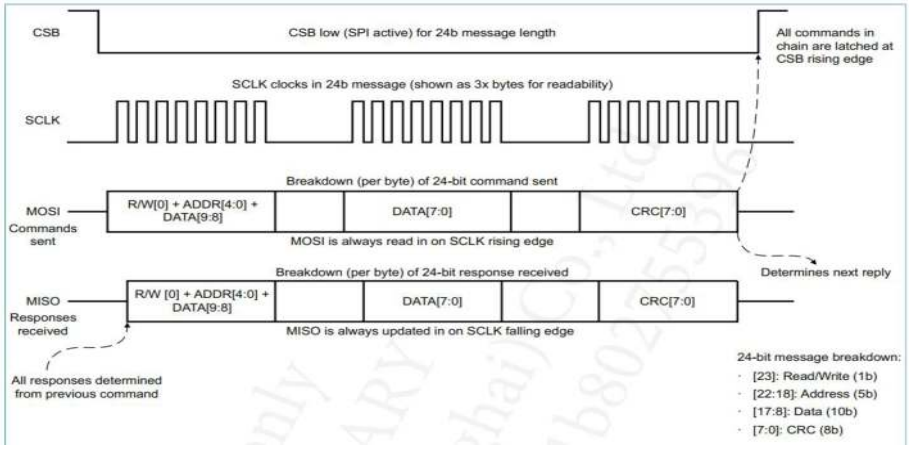


按照这个示例发出 6 组指令，也能查询到 6 组驱动的状态。其顺序是 W_L -> W_H ->V_L -> V_H -> U_L -> U_H。

SPI 数据帧为 24Bit, SPI 具体协议，数据帧格式如下：



- SPI MOSI 数据在 SCLK 上升沿读取
- SPI MISO 数据在 SCLK 下降沿变化
- SPI 通讯是 MSB 优先
- SPI 数据帧是 24Bit



SPI 需要 CRC 校验，24Bit 里的后 8 位为 CRC 校验码，其多项式为（100101111，0x2F），种子码 0x42。

SPI 寄存器：

SPI COMMANDS		Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC [7:0]
Name	**Description**	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
MODE1	Operating Mode 1	0/1	0x00	AOUT	SEGDRV	AMC	TEMPSNS	SSD	2LTO	ACTCLMP	DESAT	SCSNS	OCSNS	—
MODE2	Operating Mode 2	0/1	0x01	—	—	—	FSISOEN	—	—	BIST	CONFIG_EN	RESET	—	—
CONFIG1	Configuration 1	0/1	0x02	UV_DIS	UV_TH [2]	UV_TH [1]	UV_TH [0]	OCTH [2]	OCTH [1]	OCTH [0]	OCFILT [2]	OCFILT [1]	OCFILT [0]	—
CONFIG2	Configuration 2	0/1	0x03	—	2LTOV [2]	2LTOV [1]	2LTOV [0]	SCTH [2]	SCTH [1]	SCTH [0]	SCFILT [2]	SCFILT [1]	SCFILT [0]	—
CONFIG3	Configuration 3	0/1	0x04	—	SEGDRVDLY[2]	SEGDRVDLY[1]	SEGDRVDLY[0]	SSD_CUR [2]	SSD_CUR [1]	SSD_CUR [0]	SSDT [2]	SSDT [1]	SSDT [0]	—
CONFIG4	Configuration 4	0/1	0x05	DESAT_LEB [1]	DESAT_LEB [0]	AOUT_SEL [2]	AOUT_SEL [1]	AOUT_SEL [0]	IDESAT [1]	IDESAT [0]	DESAT_TH [2]	DESAT_TH [1]	DESAT_TH [0]	—
CONFIG5	Configuration 5	0/1	0x06	DEADT [3]	DEADT [2]	DEADT [1]	DEADT [0]	AOUTCONF [2]	AOUTCONF [1]	AOUTCONF [0]	COMERRCONF [2]	COMERRCONF [1]	COMERRCONF [0]	—
CONFIG6	Configuration 6	0/1	0x07	INTBFS	—	—	—	WDTO [1]	WDTO [0]	VGEMONDLY [3]	VGEMONDLY [2]	VGEMONDLY [1]	VGEMONDLY [0]	—
OT_TH	Config OT Threshold	0/1	0x08	OT_TH [9]	OT_TH [8]	OT_TH [7]	OT_TH [6]	OT_TH [5]	OT_TH [4]	OT_TH [3]	OT_TH [2]	OT_TH [1]	OT_TH [0]	—
OTW_TH	Config OT Warn Thresh	0/1	0x09	OTW_TH [9]	OTW_TH [8]	OTW_TH [7]	OTW_TH [6]	OTW_TH [5]	OTW_TH [4]	OTW_TH [3]	OTW_TH [2]	OTW_TH [1]	OTW_TH [0]	—
STATUS1	Status 1	0/1	0x0A	VCCOV	VCCREGUV	VSUPOV	OTSD_IC	OTSD	OTW	CLAMP	DESAT	SC	OC	—
MSK1	Status Mask 1	0/1	0x0B	VCCOVM	VCCREGUVM	VSUPOVM	—	OTSDM	OTWM	CLAMPM	—	—	—	—
STATUS2	Status 2	0/1	0x0C	BIST_FAIL	VDD_UVOV	DTFLT	SPIERR	CONFCRCERR	VGE_FLT	WDOG_FLT	COMERR	VREF_UV	VEE	—
MSK2	Status Mask 2	0/1	0x0D	—	—	DTFLTM	SPIERRM	CONFCRCERRM	VGE_FLTM	WDOG_FLTM	COMERRM	VREF_UVM	VEEM	—
STATUS3	Status 3	0/1	0x0E	—	—	—	FSISO	PWM	PWMALT	FSSTATE	FSENB	INTB	VGE	—
-	Not Used	0/1	0x0F	—	—	—	—	—	—	—	—	—	—	—
REQADC	REQUEST ADC (command)	0	0x10	0	0	0	0	0	0	0	AMUX_SEL [2]	AMUX_SEL [1]	AMUX_SEL [0]	—
—	REQUEST ADC (response)	0	0x10	ADCVAL [9]	ADCVAL [8]	ADCVAL [7]	ADCVAL [6]	ADCVAL [5]	ADCVAL [4]	ADCVAL [3]	ADCVAL [2]	ADCVAL [1]	ADCVAL [0]	—
REQBIST	REQUEST BIST (command)	0	0x11	0	0	0	0	0	0	0	0	0	0	—
—	REQUEST BIST (response)	0	0x11	REQBIST [9]	REQBIST [8]	REQBIST [7]	REQBIST [6]	REQBIST [5]	REQBIST [4]	REQBIST [3]	REQBIST [2]	REQBIST [1]	REQBIST [0]	—

SPI 实例：

1. 读取 6 路 status1 寄存器：

发送 16 进制数 0x 2800A6 2800A6 2800A6 2800A6 2800A6 2800A6

读到 16 进制数 0x 2800A6 2800A6 2800A6 2800A6 2800A6 2800A6

表示 status1 状态正常，没有故障。

2. 设置开启 DESAT 保护功能:

发送 16 进制数 0x 840407 840407 840407 840407 840407 840407 开启 config 模式

发送 16 进制数 0x 80B79D 80B79D 80B79D 80B79D 80B79D 80B79D 开启 DESAT 功能

发送 16 进制数 0x 8400BB 8400BB 8400BB 8400BB 8400BB 8400BB 关闭 config 模式

详细寄存器信息表（参考 NXP GD3100 芯片 datasheet）：

Mode1 register

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x00	AOUT	SEGDRV	AMC	TEMPSNS	SSD	2LTO	ACTCLMP	DESAT	SCSNS	OCSNS	—
Default	—	—	0	0	1	0	1	1	0	0	1	1	—

Mode1 register description

Bit	Bit description	Logic 0	Logic 1
AOUT	Logic 0 is normal operation. Logic 1 enables dual signal monitoring	The HV domain reports IGBT temperature only. AOUT pin is continuously running at 4.0 kHz, with its duty cycle a function of the Temp Sensor ADC result (10 % = 000hex, 90 % = 3FFhex).	The HV domain reports AMUX value as well as IGBT temperature. AOUT encodes Temp sense followed by whatever is selected in the AMUX configuration bits. Signals appear at AOUT alternatively at 4.0 kHz and 6.0 kHz periods.

Bit	Bit description	Logic 0	Logic 1
SEGDRV	Segmented drive enable/disable bit	Segmented drive feature disabled	Segmented drive feature enabled
AMC	Active Miller Clamp enable/disable bit	Active Miller Clamp feature disabled. AMC transistor will be deactivated but the AMC_th comparator is still operational.	Active Miller Clamp feature enabled
TEMPSNS	IGBT overtemperature shutdown and warning fault management enable/ disable bit	IGBT overtemperature shutdown and warning fault management disabled. I_{OT} disabled	IGBT overtemperature shutdown and warning fault management enabled. I_{OT} enabled
SSD	Soft shutdown enable/disable bit	Soft Shutdown disabled	Soft shutdown enabled
2LTO	Two Level Turn Off enable/disable bit	Two Level Turn Off disabled	Two Level Turn Off enabled
ACTCLMP	V_{CE} Active Clamping enable/disable bit	V_{CE} Active Clamping disabled	V_{CE} Active Clamping enabled
DESAT	V_{CE} DESAT fault management enable/ disable bit	V_{CE} DESAT fault management disabled	V_{CE} DESAT fault management enabled
SCSNS	IGBT short current fault management enable/disable bit	IGBT short current fault management disabled	IGBT short current fault management enabled
OCSNS	IGBT overcurrent fault management enable/disable bit	IGBT overcurrent fault management disabled	IGBT Overcurrent fault management enabled

Mode2 register

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x01	—	—	—	FSISOEN	—	—	BIST	CONFIG_EN	RESET	—	—
Default	—	—	—	—	—	1	—	—	0	0	0	—	—

Mode2 register description

Bit	Bit description	Logic 0	Logic 1
FSISOEN	FSISO enable/disable	FSISO pin is not active; pin state is ignored	FSISO pin is active. FSISO pin controls tri-state condition of gate drive.
BIST	BIST enable/disable	BIST feature is not active	Requests BIST of LV and HV domains. PWMing is disabled until BIST is complete and BIST is reset to Logic 0. IGBT is OFF during BIST.
CONFIG_EN	SPI register configuration enable/ disable	Configuration of SPI registers is disabled. Normal operation.	Enables configuration of the SPI registers. IGBT gate is OFF during configuration. CRC value of configured registers is calculated and stored on CSB rising edge when exiting CONFIGN_EN. PWMing is allowed after CONFIG_EN bit = 0. INTB pin reports faults normally.
RESET	Reset enable/disable	MC33GD3100 not in Reset. Normal operating mode.	MC33GD3100 in Reset. All configuration registers are set to default values. PWMing is disabled. Configuration is disabled. IGBT Is OFF. INTB = 0

CONFIG1 register

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x02	UV_DIS	UV_TH [2]	UV_TH [1]	UV_TH [0]	OCTH [2]	OCTH [1]	OCTH [0]	OCFILT [2]	OCFILT [1]	OCFILT [0]	—
Default	—	—	0	0	1	1	0	1	1	0	1	1	—

CONFIG1 register description

Bit	Bit description
UV_DIS	The UV_DIS bit provides flexibility in how the high voltage domain responds when it recovers from a VCCREG undervoltage condition [1]
UV_TH [2:0]	VCCREG undervoltage threshold
OCTH [2:0]	Overcurrent threshold
OCFILT [2:0]	Overcurrent fault filter time

Value [2:0]	UV_TH	OCTH	OCFILT
0x00	10.0 V	0.25 V	0.5 µs
0x01	10.5 V	0.50 V	1.0 µs
0x02	11.0 V	0.75 V	1.5 µs
0x03	11.5 V	1.00 V	2.0 µs
0x04	12.0 V	1.25 V	2.5 µs
0x05	12.5 V	1.50 V	3.0 µs
0x06	13.0 V	1.75 V	3.5 µs
0x07	13.5 V	2.00 V	4.0 µs

CONFIG2 register

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x03	—	2LTOV [2]	2LTOV [1]	2LTOV [0]	SCTH [2]	SCTH [1]	SCTH [0]	SCFILT [2]	SCFILT [1]	SCFILT [0]	—
Default	—	—	—	0	1	1	0	1	0	1	0	0	—

CONFIG2 register description

Bit	Bit description
2LTOV [2:0]	2 Level Turn-off voltage
SCTH [2:0]	Short-circuit threshold voltage
SCFILT [2:0]	Short-circuit filter time. Duration of 2LTO interval.

Value [2:0]	2LTOV	SCTH	SCFILT
0x00	8.91 V	0.50 V	400 ns
0x01	9.23 V	0.75 V	500 ns
0x02	9.58 V	1.00 V	600 ns

Value [2:0]	2LTOV	SCTH	SCFILT
0x03	9.96 V	1.25 V	700 ns
0x04	10.39 V	1.50 V	800 ns
0x05	10.84 V	2.00 V	900 ns
0x06	11.35 V	2.50 V	1000 ns
0x07	11.89 V	3.00 V	1100 ns

CONFIG3 register

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x04	—	SEGDR VDLY[2]	SEGDR VDLY[1]	SEGDR VDLY[0]	SSD_ CUR [2]	SSD_ CUR [1]	SSD_ CUR [0]	SSDT [2]	SSDT [1]	SSDT [0]	—
Default	—	—	—	0	0	0	1	0	0	1	0	0	—

CONFIG3 register description

Bit	Bit description
SEGDRVDLY[2:0]	Segmented drive activation delay
SSD_CUR [2:0]	Soft shutdown current
SSDT [2:0]	Soft shutdown time

Value [2:0]	SEGDRVDLY	SSD_CUR	SSDT
0x00	20 ns	0.094 A	2000 ns
0x01	40 ns	0.186 A	3000 ns
0x02	60 ns	0.277 A	4000 ns
0x03	80 ns	0.367 A	5000 ns
0x04	100 ns	0.541 A	6000 ns
0x05	120 ns	0.704 A	7000 ns
0x06	140 ns	0.858 A	8000 ns
0x07	160 ns	0.996 A	9000 ns

CONFIG4 register

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x05	DESAT_ LEB [1]	DESAT_ LEB [0]	AOUT_ SEL [2]	AOUT_ SEL [1]	AOUT_ SEL [0]	IDESAT [1]	IDESAT [0]	DESAT_ TH [2]	DESAT_ TH [1]	DESAT_ TH [0]	—
Default	—	—	1	0	0	0	0	0	1	0	1	1	—

CONFIG4 register description

Bit	Bit description
DESAT_LEB [1:0]	Desaturation leading edge blanking time
AOUT_SEL [2:0]	AOUT_SEL is used for dual AOUT reporting mode (to select the second signal to send out in addition to IGBT temp)
IDESAT [1:0]	Charging current for desaturation detection circuitry
DESAT_TH [2:0]	V_{CE} desaturation threshold

Value [2:0]	DESAT_LEB	AOUT_SEL	IDESAT	DESAT_TH
0x00	400 ns	IGBT Temp	250 µA	3.00 V
0x01	500 ns	AMUXIN	500 µA	4.00 V
0x02	600 ns	VCC	750 µA	5.00 V
0x03	700 ns	GH Temp	1000 µA	6.00 V
0x04	—	—	—	7.00 V
0x05	—	—	—	8.00 V
0x06	—	—	—	9.00 V
0x07	—	—	—	10.00 V

CONFIG5 register

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x06	DEADT [3]	DEADT [2]	DEADT [1]	DEADT [0]	AOUTCONF [2]	AOUTCONF [1]	AOUTCONF [0]	COMERRCONF [2]	COMERR CONF[1]	COMERRCONF [0]	—
Default	—	—	1	1	1	1	0	0	0	1	1	0	—

CONFIG5 register description

Bit	Bit description
DEADT [3:0]	Mandatory PWM deadtime
AOUTCONF [2:0]	Number of TEMPSENSE ADC readings vs. AOUT_SEL readings
COMERRCONF [2:1]	Number of LV/HV domain communications errors needed to latch a COMERR fault
COMERRCONF [0]	Number of valid LV/HV domain messages is needed to decrement the error counter

Value [3:0]	DEADT	AOUTCONF [2:0]	COMERRCONF [2:1]	COMERRCONF [0]
0x00	0.5 µs	1/1	1	1
0x01	0.75 µs	1/2	4	4
0x02	1.00 µs	1/4	8	—
0x03	1.25 µs	1/8	16	—
0x04	1.50 µs	1/8	—	—
0x05	1.75 µs	1/8	—	—
0x06	2.00 µs	1/8	—	—
0x07	2.25 µs	1/8	—	—
0x08	2.50 µs	—	—	—
0x09	2.75 µs	—	—	—
0x0A	3.00 µs	—	—	—
0x0B	3.25 µs	—	—	—
0x0C	3.50 µs	—	—	—
0x0D	3.75 µs	—	—	—
0x0E	4.00 µs	—	—	—
0x0F	4.25 µs	—	—	—

CONFIG6 register

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x07	INTBFS	—	—	—	WDTO [1]	WDTO [0]	VGEMONDLY [3]	VGEMONDLY [2]	VGEMONDLY [1]	VGEMONDLY [0]	—
Default	—	—	0	—	—	—	1	1	1	1	1	1	—

CONFIG6 register description

Bit	Bit description
INTBFS [0]	This bit controls the behavior of the INTB pin in fail-safe mode. • When INTBFS = 0, then the state of FSENB does not affect INTB • When INTBFS = 1, then INTB = 0 when FSENB = 0
WDTO [1:0]	Watchdog timeout
VGEMONDLY [3:0]	PWM vs. V_{GE} monitor delay

Value [3:0]	WDTO	VGEMONDLY
0x00	260 µs	400 ns
0x01	500 µs	600 ns
0x02	1000 µs	800 ns
0x03	2000 µs	1000 ns
0x04		1200 ns
0x05		1400 ns
0x06		1600 ns
0x07		1800 ns
0x08		2000 ns
0x09		2400 ns
0x0A		2800 ns
0x0B		3200 ns
0x0C		3600 ns
0x0D		4000 ns
0x0E		4400 ns
0x0F		4800 ns

OT_TH (IGBT overtemperature threshold register)

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x08	OT_TH [9]	OT_TH [8]	OT_TH [7]	OT_TH [6]	OT_TH [5]	OT_TH [4]	OT_TH [3]	OT_TH [2]	OT_TH [1]	OT_TH [0]	—
Default	—	—	1	1	1	1	1	1	1	1	1	1	—

OT_TH (IGBT overtemperature threshold register) description

Bits	Bit description
OT_TH [9:0]	Overtemperature shutdown threshold

Value [9:0]	OT_TH value
OT_TH [9:0]	OT_TH [9:0] * 5.0 V / 1024

OTW_TH (IGBT overtemperature warning threshold register)

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x09	OTW_TH [9]	OTW_TH [8]	OTW_TH [7]	OTW_TH [6]	OTW_TH [5]	OTW_TH [4]	OTW_TH [3]	OTW_TH [2]	OTW_TH [1]	OTW_TH [0]	—
Default	—	—	1	1	1	1	1	1	1	1	1	1	—

OTW_TH (IGBT overtemperature warning threshold register) description

Bits	Bit description
OTW_TH [9:0]	Overtemperature warning threshold

Value [9:0]	OTW_TH value
OTW_TH [9:0]	OTW_TH [9:0] * 5.0 V / 1024

STATUS1 register

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x0A	VCCOV	VCCREGUV	VSUPOV	OTSD_IC	OTSD	OTW	CLAMP	DESAT	SC	OC	—
Default	—	—	0	0	0	0	0	0	0	0	0	0	—

STATUS1 register description

Bit	Logic 1 indicates:	Fault latched	PWMing disabled	IGBT turn off method
VCCOV	VCC overvoltage	yes	yes, GL = 1, AMC = 1 if enabled	normal
VCCREGUV [1]	VCCREG undervoltage	yes	yes, GL = 1, AMC = 1 if enabled	normal
VSUPOV	VSUP overvoltage	yes	yes, GL = 1, AMC = 1 if enabled	normal
OTSD_IC	Overtemperature shutdown of LV domain or HV domain	yes	yes, GL = 1, AMC = 1 if enabled	normal
OTSD	Overtemperature shutdown of IGBT	yes	yes, GL = 1, AMC = 1 if enabled	normal
OTW	Overtemperature warning of IGBT	yes	no	not turned off
CLAMP [2]	V_{CE} clamp event	yes	yes, GL = 1, AMC = 1 if enabled	I_{SSD} defaults to lowest setting
DESAT	V_{CE} desaturation event	yes	yes, GL = 1, AMC = 1 if enabled	SSD, 2LTO if enabled
SC	IGBT short-circuit	yes	yes, GL = 1, AMC = 1 if enabled	SSD, 2LTO if enabled
OC	IGBT overcurrent	yes	no	SSD, if enabled

MSK1 register

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x0B	VCCOVM	VCCREGUVM	VSUPOVM	—	OTSDM	OTWM	CLAMPM	—	—	—	—
Default	—	—	1	1	0	—	1	1	1	—	—	—	—

MSK1 register description

Bit	Logic 0 = masked	Logic 1 = not masked
VCCOVM	PWMing remains enabled, fault not latched or reported	PWM disabled. GL = 1, AMC = 1 if enabled
VCCREGUVM [1]	PWMing remains enabled, fault not latched or reported	PWM disabled. GL = 1, AMC = 1 if enabled
VSUPOVM	PWMing remains enabled, fault not latched or reported	PWM disabled. GL = 1, AMC = 1 if enabled
OTSD_ICM[2]	no mask	no mask
OTSDM	PWMing remains enabled, OTSD fault not latched or reported. Temp reported in ADCVAL and AOUT.	PWM disabled. GL = 1, AMC = 1 if enabled
OTWM	PWMing remains enabled, OTW fault not latched or reported. Temp reported in ADCVAL	PWM enabled
CLAMPM	PWMing remains enabled, fault not latched or reported	PWM disabled. GL = 1, AMC = 1 if enabled
DESATM	no mask	no mask
SCM	no mask	no mask
OCM	no mask	PWM enabled

STATUS2 register

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x0C	BIST_FAIL	VDD_UVOV	DTFLT	SPIERR	CONFCRCERR	VGE_FLT	WDOG_FLT	COMERR	VREF_UV	VEE	—
Default	0	—	0	0	0	0	0	0	0	0	0	0	—

STATUS2 register description

Bit	Logic 1 indicates:	Fault latched	PWMing disabled	IGBT turn OFF method
BIST_FAIL[1]	BIST failure	yes	yes, GL = 1, AMC = 1 if enabled	normal
VDD_UVOV[2]	VDD out of range	yes	yes, GL = 1, AMC = 1 if enabled	normal
DTFLT	PWM deadtime violation	yes	no	—
SPIERR	SPI framing or CRC error	yes	no	—
CONFCRCERR	LV domain or HV domain detected a CRC change in its CONFIG registers	yes	yes, GL = 1, AMC = 1 if enabled	normal
VGE_FLT	LV domain detected that V_{GE} is not tracking commanded state.	yes	yes, GL = 1, AMC = 1 if enabled	normal
WDOG_FLT	LV domain or HV domain detects a loss of LV/HV domain communication	yes	yes, GL = 1, AMC = 1 if enabled	normal
COMERR	LV/HV domain communications CRC error or framing error	yes	yes, GL = 1, AMC = 1 if enabled	normal
VREF_UV[3]	VREF out of range	yes	yes, GL = 1, AMC = 1 if enabled	normal
VEE	VEE out of range	yes	yes, GL = 1, AMC = 1 if enabled	normal

MSK2 register

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x0D	—	—	DTFLTM	SPIERRM	CONFCRCERRM	VGE_FLTM	WDOG_FLTM	COMERRM	VREF_UVM	VEEM	—
Default	—	—	0	0	1	1	1	0	1	1	1	0	—

MSK2 register description

Bit	Description	Logic 0 = masked	Logic 1 = not masked
DTFLTM	Deadtime fault mask	PWMing remains enabled, fault not latched or reported, programmed PWM deadtime is enforced	PWM enabled
SPIERRM	SPI CRC or framing error fault mask	PWMing remains enabled, fault not latched or reported	PWM enabled
CONFCRCERRM	LV or HV domain CONF register CRC error mask	PWMing remains enabled, fault not latched or reported	PWM disabled. GL = 1, AMC = 1 if enabled
VGE_FLTM	VGE monitor error mask	PWMing remains enabled, fault not latched or reported	PWM disabled. GL = 1, AMC = 1 if enabled
WDOG_FLTM[1]	Watchdog fault mask	PWMing remains enabled, fault not latched or reported, periodic REQADC continues	PWM disabled. GL = 1, AMC = 1 if enabled
COMERRM	Internal communications fault mask	PWMing remains enabled, fault not latched or reported	PWM disabled. GL = 1, AMC = 1, if enabled
VREF_UVM[2]	VREF out of range mask	PWMing remains enabled, fault not latched or reported	PWM disabled. GL = 1, AMC = 1 if enabled
VEEM	VEE out of range mask	PWMing remains enabled, fault not latched or reported	PWM disabled. GL = 1, AMC = 1 if enabled

STATUS3 register

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Name/Value	0/1	0x0E	—	—	—	FSISO	PWM	PWMALT	FSSTATE	FSENB	INTB	VGE	—
Default	—	—	—	—	—	—	—	—	—	—	—	—	—

STATUS3 register description

Bits FSISO, PWM, PWMALT, FSSTATE, FSENB, INTB and VGE merely report the high/low state of that pin. The MCU can monitor these bits to check circuit integrity, if desired.

Bit	Logic 1 indicates:
FSISO	FSISO = Logic 1
PWM	PWM = Logic 1
PWMALT	PWMALT = Logic 1
FSSTATE	FSSTATE = Logic 1
FSENB	FSENB = Logic 1
INTB	INTB = Logic 1
VGE	VGE = Logic 1

Request ADC Register (REQADC)

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
Command	0	0x10	0	0	0	0	0	0	0	AMUX_ SEL [2]	AMUX_ SEL [1]	AMUX_ SEL [0]	—
Response	0	0x10	ADCVAL [9]	ADCVAL [8]	ADCVAL [7]	ADCVAL [6]	ADCVAL [5]	ADCVAL [4]	ADCVAL [3]	ADCVAL [2]	ADCVAL [1]	ADCVAL [0]	—

Request ADC Register (REQADC) description

Bit	Bit description
AMUX_SEL [2:0]	Selects which AMUX signal is sent to the ADC when the SPI requests an ADC conversion
ADCVAL [9:0]	ADC value of the temp sense or AMUX reading

AMUX_SEL [2:0]	AMUX_SEL
0x00	IGBT Temp
0x01	AMUXIN
0x02	VCC
0x03	HV domain Temp

ADCVAL [9:0]	ADCVAL value
ADCVAL [9:0]	ADCVAL [9:0] * 5.0 V / 1024

REQBIST (Request BIST Message)

	Rb/W	ADDR [4:0]	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CRC
Bit #	[23]	[22:18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
REQUEST BIST (command)	0	0x11	0	0	0	0	0	0	0	0	0	0	—
REQUEST BIST (response)	0	0x11	REQBIST [9]	REQBIST [8]	REQBIST [7]	REQBIST [6]	REQBIST [5]	REQBIST [4]	REQBIST [3]	REQBIST [2]	REQBIST [1]	REQBIST [0]	—

REQBIST (Request BIST Message) description

Bit	Logic 1 indicates BIST failure in:
REQBIST [9]	DATA _IN, DATA_OUT communications link
REQBIST [8]	LBIST LV domain, logic state machine, timers and combinational logic
REQBIST [7]	LBIST HV domain, logic state machine, timers and combinational logic
REQBIST [6]	Oscillator failure (LV or HV domains)
REQBIST [5]	DESAT comparator
REQBIST [4]	ISENSE short-circuit and overcurrent comparators
REQBIST [3]	Overtemperature protection (LV or HV domains)
REQBIST [2]	ADC
REQBIST [1]	LV domain power management diagnostics, OV/UV monitors
REQBIST [0]	HV domain power management diagnostics, OV/UV monitors