

CT430

XtremeSense® TMR Ultra-Low Noise, <1% Total Error Current Sensor

Features

- Integrated Contact Current Sensing for Low to Medium Current Ranges:
 - 0 A to +20 A
 - -20 A to +20 A
 - 0 A to +30 A
 - -30 A to +30 A
 - 0 A to +50 A
 - -50 A to +50 A
 - 0 A to +65 A
 - -65 A to +65 A
- Integrated Current Carrying Conductor (CCC)
- Linear Analog Output Voltage
- Total Error Output $\leq \pm 1.0\%$ FS, -40°C to $+125^{\circ}\text{C}$
- 1 MHz Bandwidth
- Response Time: ~ 300 ns
- UL/IEC 62387 Certification
 - Rated Isolation Voltage: >5 kV_{RMS}
 - Working Voltage for Basic Isolation: >1287 V_{RMS}
 - Working Voltage for Reinforced Isolation: >647 V_{RMS}
- IEC 61000-4-5 Certification
- Low Noise: 9 mA_{RMS} to 15 mA_{RMS} @ f_{BW} = 100 kHz
- Reference Voltage Output for AC/DC Current Measurements
- VOUT – VREF $< \pm 1.0\%$ FS, -40°C to $+125^{\circ}\text{C}$
- Immunity to Common Mode Fields: -54 dB
- Supply Voltage: 4.75 V to 5.50 V
- Over-Current Detection (OCD™)
 - Out of Range Currents
- AEC-Q100 Grade 1 (Under Qualification)
- 16-Lead SOIC-Wide Package

Applications

- Solar/Power Inverters
- UPS, SMPS and Telecom Power Supplies
- Battery Management Systems
- Motor Control
- White Goods
- Power Utility Meters
- Over-Current Fault Protection

Product Description

The CT430 is a high bandwidth and ultra-low noise integrated contact current sensor that uses Crocus Technology's patented XtremeSense® TMR technology to enable high accuracy current measurements for many consumer, enterprise, and industrial applications. It supports eight (8) current ranges where the integrated current carrying conductor (CCC) will handle up to 65 A of current and generates a current measurement as a linear analog output voltage. It achieves a total output error of less than $\pm 1.0\%$ full-scale (FS) over voltage and the full temperature range.

It has about a 300 ns output response time while the current consumption is about 6.0 mA and is immune to common mode fields. The CT430 has an integrated over-current detection (OCD) circuitry to identify out of range currents (OCD) with the result outputted to the fault-bar (FLT) pin. The FLT is an open drain, active LOW digital signal that is activated by the CT430 to alert, for example a microcontroller that a fault condition has occurred.

The CT430 is offered in an industry standard 16-lead SOIC-Wide package that is "green" and RoHS compliant.

Part Ordering Information

Part Number	Auto Grade	Operating Temperature Range	Current Range	Package	Packing Method
CT430-ESWF20DR	-	-40°C to +85°C	0 A to +20 A	16-lead SOIC-Wide 10.21 x 10.31 x 2.54 mm	Tape & Reel
CT430-HSWF20DR	-	-40°C to +125°C			
CT430-ASWF20DR	Grade 1				
CT430-ESWF20MR	-	-40°C to +85°C	-20 A to +20 A		
CT430-HSWF20MR	-	-40°C to +125°C			
CT430-ASWF20MR	Grade 1				
CT430-ESWF30DR	-	-40°C to +85°C	0 A to +30 A		
CT430-HSWF30DR	-	-40°C to +125°C			
CT430-ASWF30DR	Grade 1				
CT430-ESWF30MR	-	-40°C to +85°C	-30 A to +30 A		
CT430-HSWF30MR	-	-40°C to +125°C			
CT430-ASWF30MR	Grade 1				
CT430-ESWF50DR	-	-40°C to +85°C	0 A to +50 A		
CT430-HSWF50DR	-	-40°C to +125°C			
CT430-ASWF50DR	Grade 1				
CT430-ESWF50MR	-	-40°C to +85°C	-50 A to +50 A		
CT430-HSWF50MR	-	-40°C to +125°C			
CT430-ASWF50MR	Grade 1				
CT430-ESWF65DR	-	-40°C to +85°C	0 A to +65 A		
CT430-HSWF65DR	-	-40°C to +125°C			
CT430-ASWF65DR	Grade 1				
CT430-ESWF65MR	-	-40°C to +85°C	-65 A to +65 A		
CT430-HSWF65MR	-	-40°C to +125°C			
CT430-ASWF65MR	Grade 1				

Evaluation Board Ordering Information

Part Number	Current Range	Operating Temperature Range
CTD430-20DC	0 A to +20 A	-40°C to +125°C
CTD430-20AC	-20 A to +20 A	
CTD430-30DC	0 A to +30 A	
CTD430-30AC	-30 A to +30 A	
CTD430-50DC	0 A to +50 A	
CTD430-50AC	-50 A to +50 A	
CTD430-65DC	0 A to +65 A	
CTD430-65AC	-65 A to +65 A	

Block Diagram

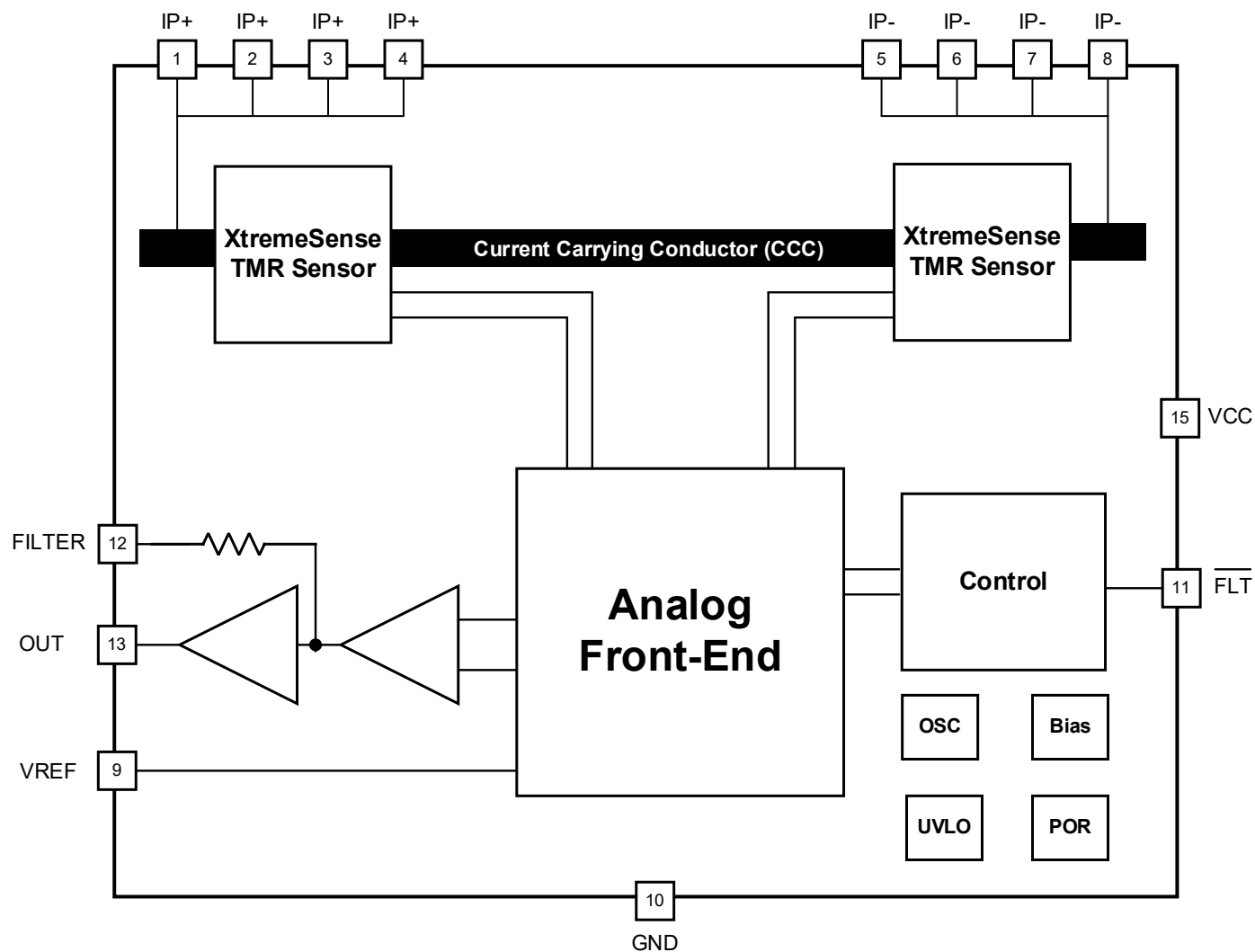


Figure 1. CT430 Functional Block Diagram for 16-lead SOIC-Wide Package

Application Diagram

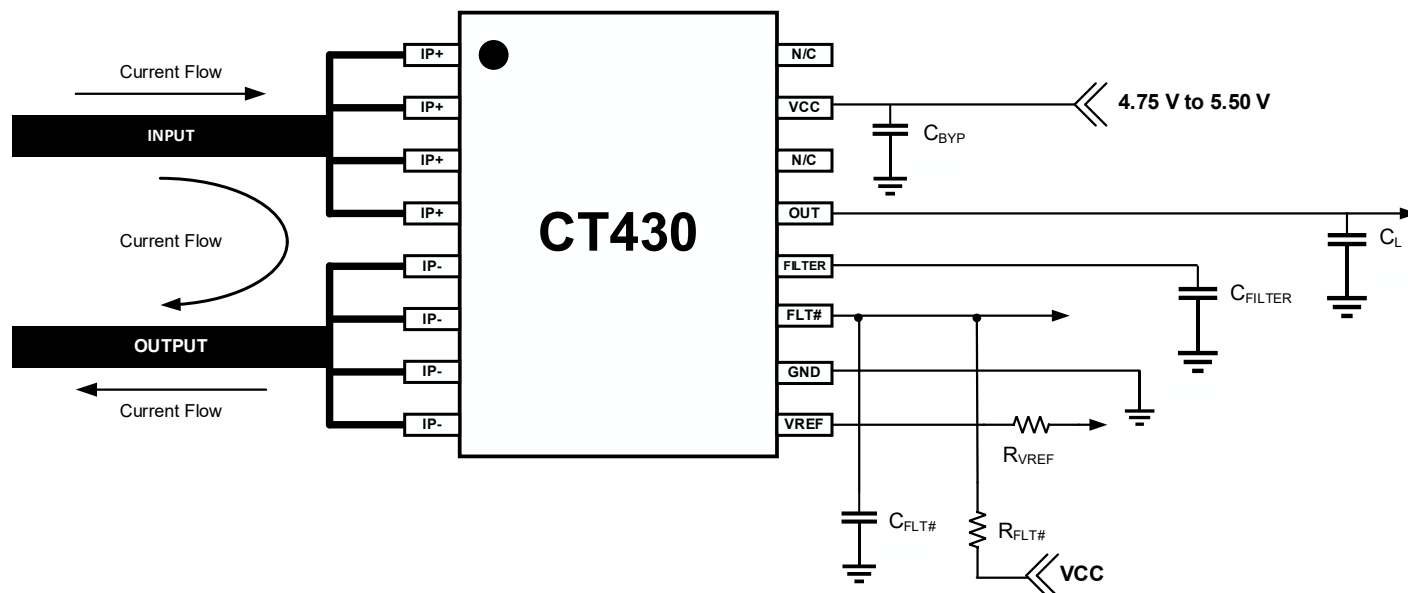


Figure 2. CT430 Application Block Diagram

Table 1. Recommended External Components

Component	Description	Vendor & Part Number	Parameter	Min.	Typ.	Max.	Unit
C_{BYP}	1.0 μ F, X5R or Better	Murata GRM155C81A105KA12	C1		1.0		μ F
C_{FILTER}	Various, X5R or Better	Murata	C2		Table 2		pF
$C_{FLT\#}$	1.0 pF, X5R or Better	Murata GRM0335C1E102JA01	C3		1.0		nF
$R_{FLT\#}$	100 k Ω Pull-up Resistor	Various	R1		100		k Ω
R_{VREF}	10 k Ω Resistor	Various	R2		10		k Ω

CT430 Pin Configuration

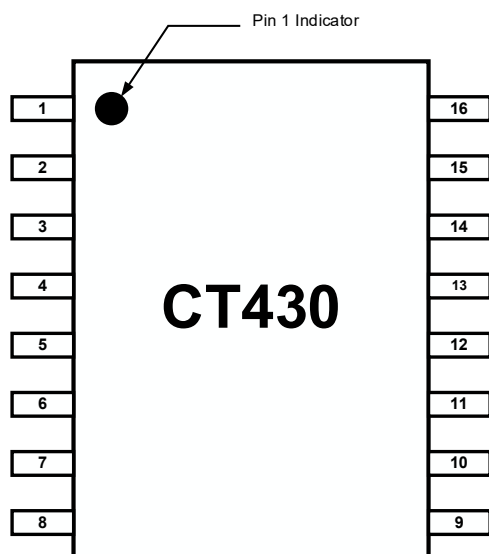


Figure 3. CT430 Pin-out Diagram for 16-lead SOIC-Wide Package (Top-Down View)

Pin Definition

Pin #	Pin Name	Pin Description
1	IP+	Terminal for primary conductor (positive).
2		
3		
4		
5	IP-	Terminal for primary conductor (negative).
6		
7		
8		
9	VREF	Reference voltage output. If not used, then do not connect.
10	GND	Ground.
11	$\overline{\text{FLT}}$	Active LOW output fault signal (open drain output) to indicate that the following parameters are outside of normal operational bounds: - Over-Current Detection - UVLO If not used, then a 1.0 nF capacitor must be connected from the pin to ground.
12	FILTER	Filter pin to improve noise performance by connecting an external capacitor to set the cut-off frequency. If not used, then do not connect the pin (No Connect).
13	OUT	Analog output voltage that represents the measured current.
14	N/C	No connect.
15	VCC	Supply voltage.
16	N/C	No connect.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the CT430 and may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V _{CC}	Supply Voltage		-0.3	6.0	V
V _{I/O}	Analog Input/Output Pins Maximum Voltage		-0.3	V _{CC} + 0.3*	V
I _{CC} (MAX)	Current Carrying Conductor, T _A = +25°C			70	A
V _{SURGE}	Dielectric Surge Strength Test Voltage	IEC 61000-4-5 : Tested ±5 Pulses at 2/60 seconds, 1.2 μs (rise) and 50 μs (width)	6.0		kV
I _{SURGE}	Surge Strength Test Current	Tested ±5 Pulses at 3/60 seconds, 8.0 μs (rise) and 20 μs (width)	3.0		kA
ESD	Electrostatic Discharge Protection Level	Human Body Model (HBM) per JESD22-A114	±2.0		kV
		Charged Device Model (CDM) per JESD22-C101	±0.5		
T _J	Junction Temperature		-40	+150	°C
T _{STG}	Storage Temperature		-65	+155	°C
T _L	Lead Soldering Temperature, 10 Seconds			+260	°C

*The lower of V_{CC} + 0.3 V or 6.0 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual operation of the CT430. Recommended operating conditions are specified to ensure optimal performance to the specifications. Crocus Technology does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage Range		4.75	5.00	5.50	V
V _{OUT}	OUT Voltage Range		0		V _{CC}	V
I _{OUT}	OUT Current				±1.0	mA
T _A	Operating Ambient Temperature	Industrial	-40	+25	+85	°C
		Extended Industrial	-40	+25	+125	
		Automotive	-40	+25	+125	

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout and is determined in accordance to JEDEC standard JESD51 for a four (4) layer 2s2p FR-4 printed circuit board (PCB) with 2 oz. of copper (Cu) for 20 A or 30 A and 4 oz. of copper (Cu) or more for 50 A or 65 A. Special attention must be paid not to exceed junction temperature T_J(MAX) at a given ambient temperature T_A.

Symbol	Parameter	Min.	Typ.	Max.	Unit
θ _{JA_SOICW}	Junction-to-Ambient Thermal Resistance, SOICW-16		119	144	°C/W
θ _{JC_SOICW}	Junction-to-Case Thermal Resistance, SOICW-16		86	112	°C/W

Isolation Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{ISO}	Rated Isolation Voltage	Agency Tested per IEC 62368* for 60 seconds. Production Tested at V _{ISO} for 1 second per IEC 62368.	5.0	kV _{RMS}
		Agency Tested per UL1577 for 60 seconds. Production Tested at V _{ISO} for 1 second per UL1577.	5.0	kV _{RMS}
V _{WORK_ISO}	Working Voltage for Basic Isolation	Tested per per IEC 62368*	1820	V _{PK}
			1287	V _{RMS}
V _{WORK_RI}	Working Voltage for Reinforced Isolation	Tested per IEC 62368*	915	V _{PK}
			647	V _{RMS}
d _{CR}	Creepage Distance	Minimum Distance Along Package Body from IP Pins to I/O Pins	9.21	mm
d _{CL}	Clearance Distance	Minimum Distance Through Air from IP Pins to I/O Pins	8.79	mm
d _{ISO}	Distance Through Isolation	Minimum Internal Distance Through Isolation	110	μm
CTI	Comparative Tracking Index	Material Group II	400 to 599	V

*IEC 62368 is the succeeding standard to IEC 60950-1 (Edition 2) for isolation testing specifications and as such it will be compliant to the latter standard.

Electrical Specifications

General Parameters

Unless otherwise specified: V_{CC} = 4.75 V to 5.50 V, T_A = -40°C to +125°C, C_{BYP} = 1.0 μF. Typical values are V_{CC} = 5.00 V and T_A = +25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supplies						
I _{CC}	Supply Current	f _{BW} = 1 MHz No load, I _P = 0 A		6.0	9.0	mA
I _{OUT}	OUT Maximum Drive Capability ⁽¹⁾	OUT covers 10% to 90% of V _{CC} span.	-1.0		+1.0	mA
C _{L_OUT}	OUT Capacitive Load ⁽¹⁾				100	pF
R _{L_OUT}	OUT Resistive Load ⁽¹⁾			100		kΩ
I _{VREF}	VREF Maximum Drive Capability ⁽¹⁾		-50		+50	μA
C _{L_VREF}	VREF Capacitive Load ⁽¹⁾				10	pF
R _{L_VREF}	VREF Resistive Load ⁽¹⁾			100		kΩ
R _{FILTER}	Internal Filter Resistance ⁽¹⁾			15		kΩ
R _{IP}	Primary Conductor Resistance ⁽¹⁾			0.5		mΩ
PSRR	Power Supply Rejection Ratio ⁽¹⁾			35		dB
SPSRR	Sensitivity Power Supply Rejection Ratio ⁽¹⁾			35		dB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OPSRR	Offset Power Supply Rejection Ratio ⁽¹⁾			40		dB
Analog Output (OUT)						
V _{OUT}	OUT Voltage Linear Range	V _{SIG_AC} = ±2.00 V V _{SIG_DC} = +4.00 V	0.50		4.50	V
V _{OUT_SAT}	Output High Saturation Voltage	V _{OUT} , T _A = +25°C,	V _{CC} – 0.30	V _{CC} – 0.25		V
CMFRR	Common Mode Field Rejection Ratio ⁽¹⁾			-54		dB
				0.5		mA/G
Reference Voltage (VREF)						
V _{REF}	Reference Voltage	DC Current (Unipolar)		0.50		V
		AC Current (Bipolar)		2.50		
Fault Output ($\overline{\text{FLT}}$)						
V _{FLT#_OL}	$\overline{\text{FLT}}$ Voltage LOW	I _{FLT#_OUT} ≤ 20 mA	0		0.5	V
I _{LEAK_FLT#}	High Impedance Output Leakage Current	V _{FLT#_OH} = V _{CC}		5		μA
RPU	$\overline{\text{FLT}}$ Pull-up Resistor			100		kΩ
Timings						
t _{ON}	Power-On Time ⁽¹⁾	V _{CC} ≥ 2.50 V		100	200	μs
t _{RISE}	Rise Time ⁽¹⁾	I _P = I _{RANGE(MAX)} , T _A = +25°C, C _L = 220 pF		200		ns
t _{RESPONSE}	Response Time ⁽¹⁾			300		ns
t _{DELAY}	Propagation Delay ⁽¹⁾			250		ns
t _{FLT#}	$\overline{\text{FLT}}$ Response Time ⁽¹⁾			250		ns
Protection						
V _{UVLO}	Under-Voltage Lockout	Rising V _{CC}		2.50		V
		Falling V _{CC}		2.45		V
V _{UV_HYS}	UVLO Hysteresis			50		mV
I _{OCD_U}	Over-Current Detection (OCD) for DC Current (Unipolar)	Rising I _P		1.1 × I _{RANGE(MAX)}		A
		Falling I _P		0.9 × I _{RANGE(MAX)}		
I _{OCD_B}	Over-Current Detection (OCD) for AC Current (Bipolar)	Rising I _P		±1.1 × I _{RANGE(MAX)}		A
		Falling I _P		±0.9 × I _{RANGE(MAX)}		
I _{OCD_HYS}	Over-Current Detection Hysteresis			0.2 × I _{RANGE(MAX)}		A

(1) Guaranteed by design and/or characterization; not tested in production.

Electrical Characteristics

$V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$ and $C_{BYP} = 1.0\text{ }\mu\text{F}$ (unless otherwise specified)

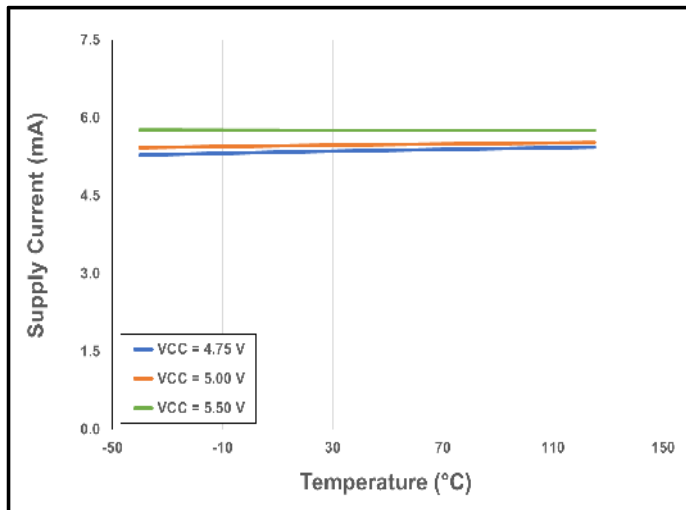


Figure 4. CT430 Supply Current vs. Temperature vs. Supply Voltage

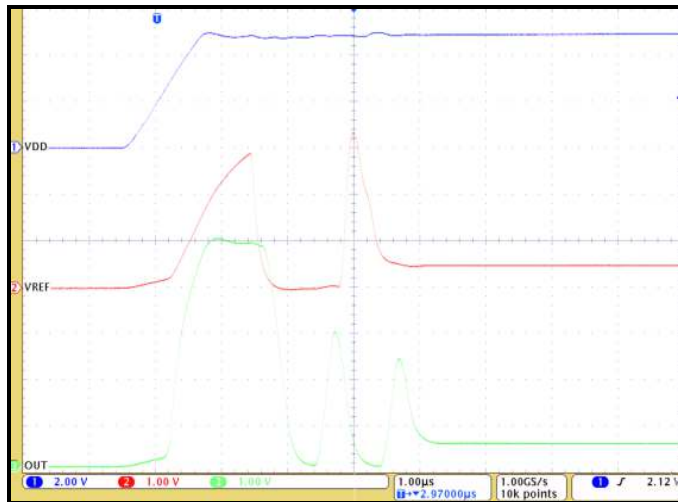


Figure 5. CT430 Startup Waveforms for $V_{OQ} = 0.50\text{ V}$ (DC Current)

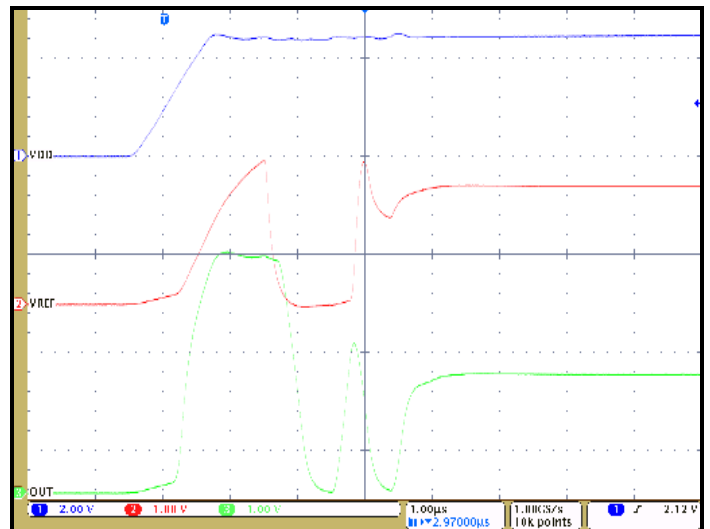


Figure 6. CT430 Startup Waveforms for $V_{OQ} = 2.50\text{ V}$ (AC Current)

Electrical Characteristics (continued)

$V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$ and $C_{BYP} = 1.0\text{ }\mu\text{F}$ (unless otherwise specified)

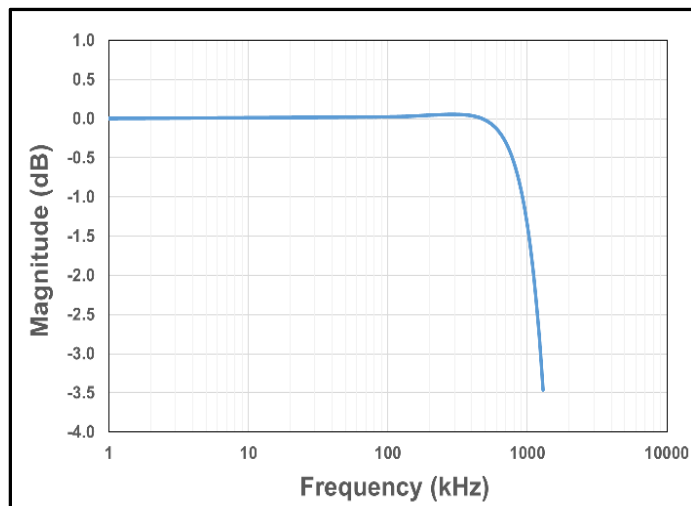


Figure 7. CT430 Bandwidth with $C_{FILTER} = 1.0\text{ pF}$

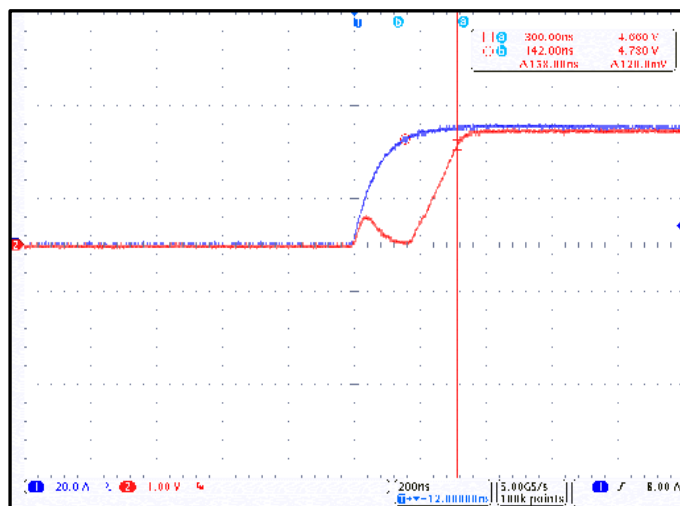


Figure 8. CT430 Response Time; $I_P = 50\text{ A}_{PK}$ and $C_L = 100\text{ pF}$ (Blue = I_{LCC} , Red = V_{OUT})

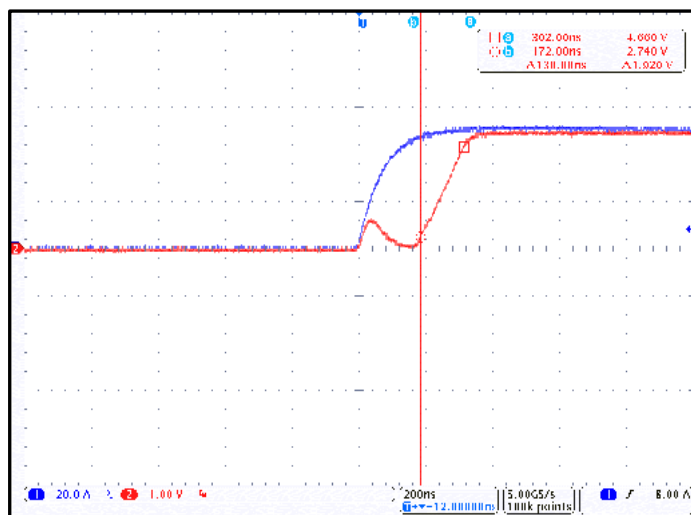


Figure 9. CT430 Rise Time; $I_P = 50\text{ A}_{PK}$ and $C_L = 100\text{ pF}$ (Blue = I_{LCC} , Red = V_{OUT})

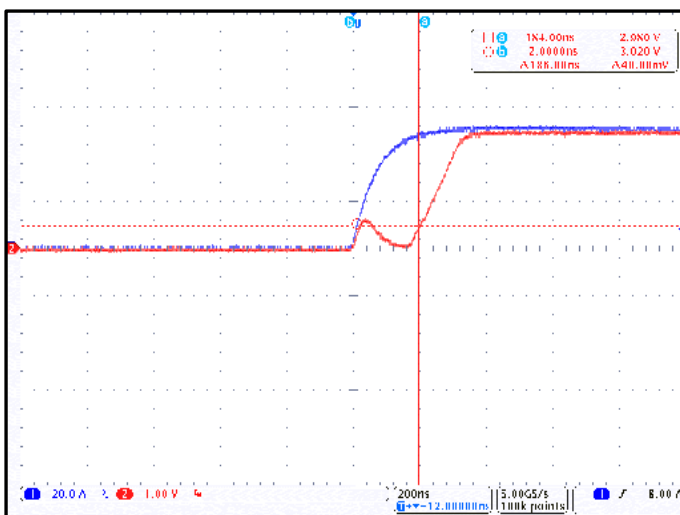


Figure 10. CT430 Propagation Delay; $I_P = 50\text{ A}_{PK}$ and $C_L = 100\text{ pF}$ (Blue = I_{LCC} , Red = V_{OUT})

Electrical Characteristics (continued)

$V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$ and $C_{BYP} = 1.0\text{ }\mu\text{F}$ (unless otherwise specified)

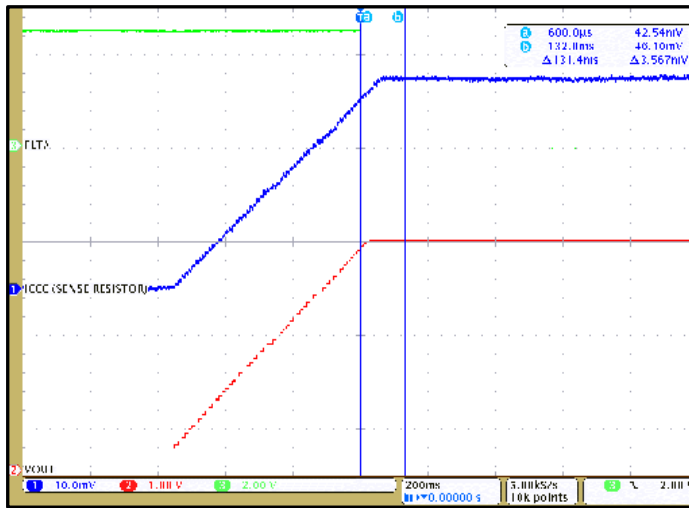


Figure 11. CT430 OCD enabled at 110% of +50 A_{DC} and FLT# is LOW



Figure 12. CT430 OCD disabled at 90% of +50 A_{DC} and FLT# is HIGH

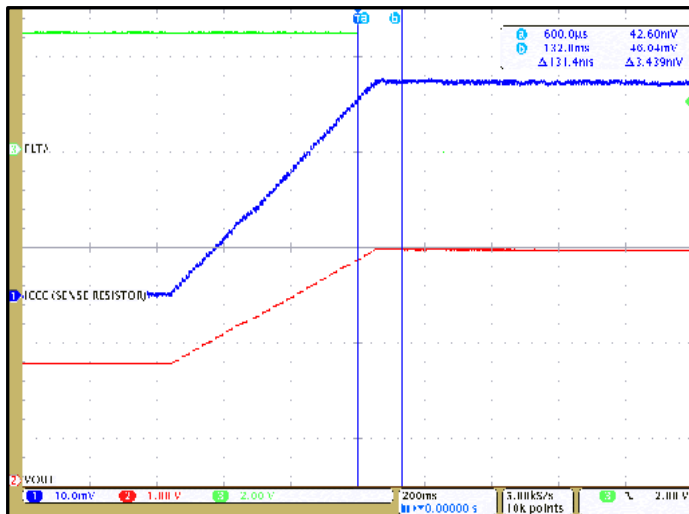


Figure 13. CT430 OCD enabled at +110% of +50 A_{PK} and FLT# is LOW

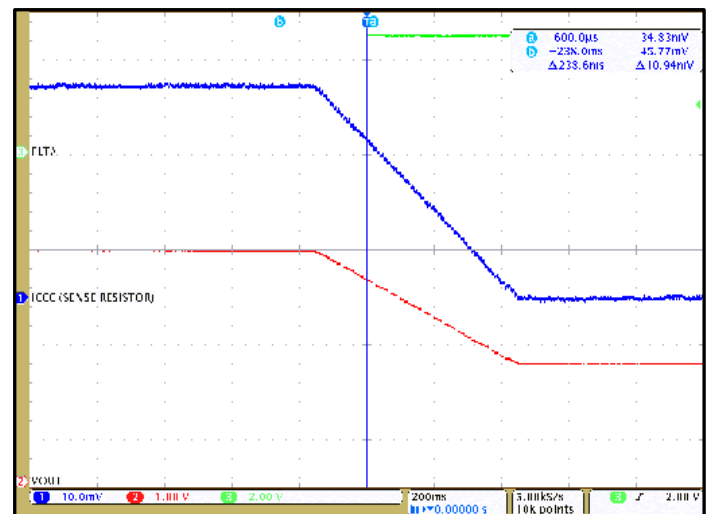


Figure 14. CT430 OCD disabled at +90% of +50 A_{PK} and FLT# is HIGH

Electrical Characteristics (continued)

$V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$ and $C_{BYP} = 1.0\text{ }\mu\text{F}$ (unless otherwise specified)



Figure 15. CT430 OCD enabled at -110% of -50 A_{PK} and FLT# is LOW

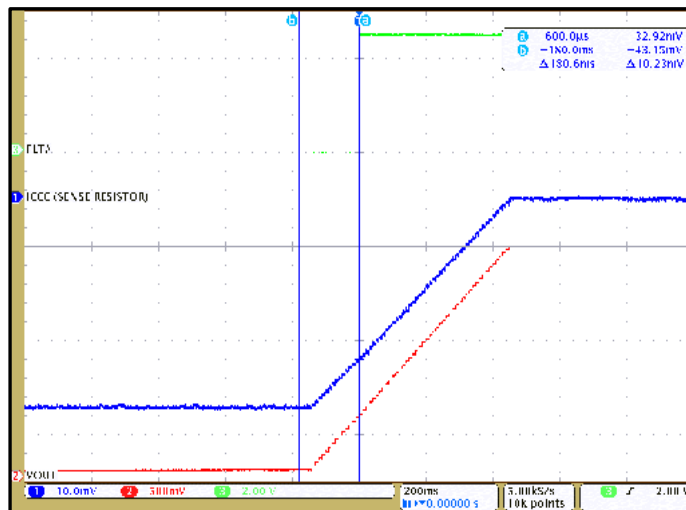


Figure 16. CT430 OCD disabled at -90% of -50 A_{PK} and FLT# is HIGH

CT430-xSWF20DR: 0 A to +20 A

Unless otherwise specified: $V_{CC} = 4.75\text{ V to }5.50\text{ V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$, $C_{BYP} = 1.0\text{ }\mu\text{F}$. Typical values are $V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{RANGE}	Current Range		0		+20	A
V _{OQ}	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	0.495	0.500	0.505	V
S	Sensitivity	I _{RANGE(MIN)} ≤ I _P ≤ I _{RANGE(MAX)}		200		mV/A
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB		1.0		MHz
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		9.0		mA _{RMS}
OUT Accuracy Performance						
E _{OUT}	Total Output Error	I _P = I _{P(MAX)}		±0.7	±1.0	% FS
E _{LIN}	Non-Linearity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.1		% FS
E _{SENS}	Sensitivity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.7		% FS
V _{OFFSET}	Offset Voltage ⁽¹⁾	I _P = 0 A, T _A = -40°C to +125°C		±12.5		mV
				±0.3		% FS
V _{OUT} – V _{REF} Accuracy Performance						
E _{OUT-VREF}	V _{OUT} – V _{REF} Error	I _P = I _{P(MAX)} , V _{CC} = 5.0 V T _A = -40°C to +125°C			±1.0	% FS
V _{OUT} - V _{REF}	OUT – V _{REF} Offset Voltage	V _{CC} = 5.0 V T _A = -40°C to +125°C		±5.0		mV
Lifetime Drift						
E _{TOT_DRIFT}	Total Output Error Lifetime Drift ⁽¹⁾	I _P = I _{P(MAX)}		±1.0		% FS

(1) Guaranteed by design and characterization; not tested in production.

Electrical Characteristics for CT430-xSWF20DR

$V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$ and $C_{BYP} = 1.0\text{ }\mu\text{F}$ (unless otherwise specified)

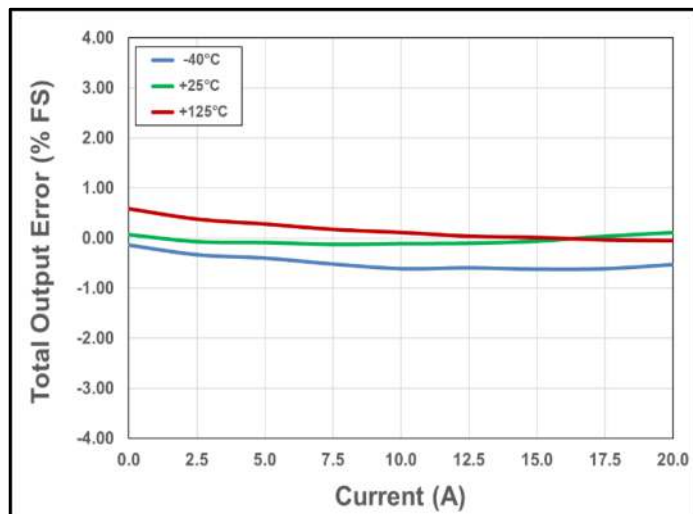


Figure 17. Total Output Error vs. Current vs. Temperature

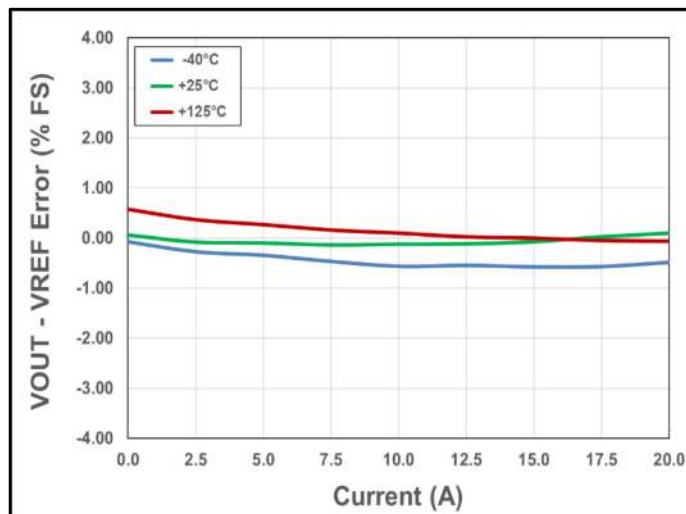


Figure 18. VOUT - VREF Error vs. Current vs. Temperature

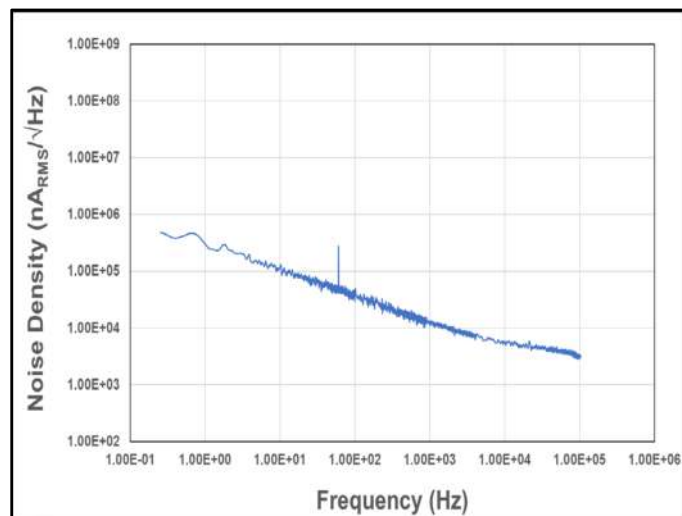


Figure 19. Noise Density vs. Frequency

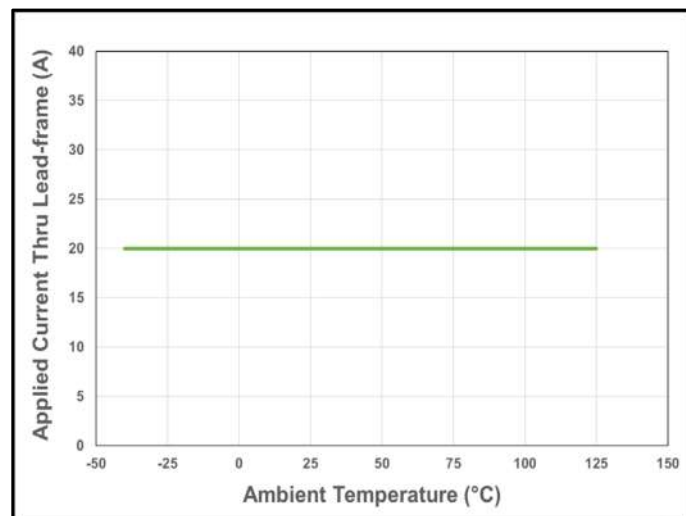


Figure 20. CT430 Current De-rating Curve for 20 A_{DC}

CT430-xSWF20MR: -20 A to +20 A

Unless otherwise specified: $V_{CC} = 4.75\text{ V to }5.50\text{ V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$, $C_{BYP} = 1.0\text{ }\mu\text{F}$. Typical values are $V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{RANGE}	Current Range		-20		+20	A
V _{OQ}	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	2.495	2.500	2.505	V
S	Sensitivity	I _{RANGE(MIN)} ≤ I _P ≤ I _{RANGE(MAX)}		100		mV/A
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB		1.0		MHz
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		10.0		mA _{RMS}
OUT Accuracy Performance						
E _{OUT}	Total Output Error	I _P = I _{P(MAX)}		±0.5	±1.0	% FS
E _{LIN}	Non-Linearity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.1		% FS
E _{SENS}	Sensitivity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.5		% FS
V _{OFFSET}	Offset Voltage ⁽¹⁾	I _P = 0 A, T _A = -40°C to +125°C		±7.0		mV
				±0.2		% FS
V _{OUT} – V _{REF} Accuracy Performance						
E _{OUT-VREF}	V _{OUT} – V _{REF} Error	I _P = I _{P(MAX)} , V _{CC} = 5.0 V T _A = -40°C to +125°C			±1.0	% FS
V _{OUT} - V _{REF}	OUT – V _{REF} Offset Voltage	V _{CC} = 5.0 V T _A = -40°C to +125°C		±5.0		mV
Lifetime Drift						
E _{TOT_DRIFT}	Total Output Error Lifetime Drift ⁽¹⁾	I _P = I _{P(MAX)}		±1.0		% FS

(1) Guaranteed by design and characterization; not tested in production.

Electrical Characteristics for CT430-xSWF20MR

$V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$ and $C_{BYP} = 1.0\text{ }\mu\text{F}$ (unless otherwise specified)

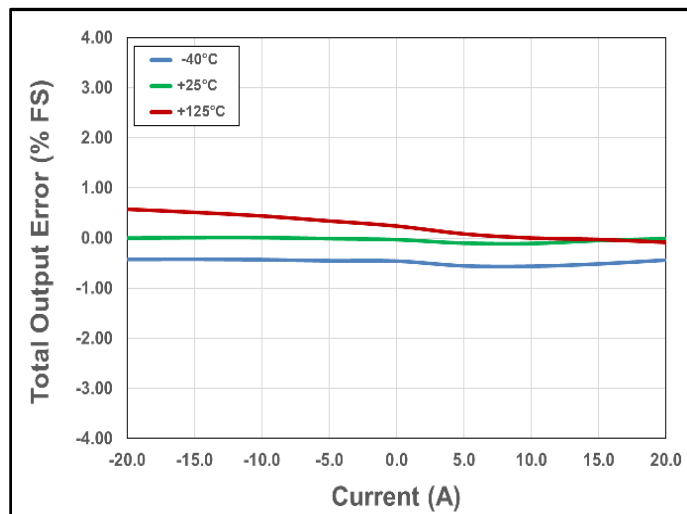


Figure 21. Total Output Error vs. Current vs. Temperature

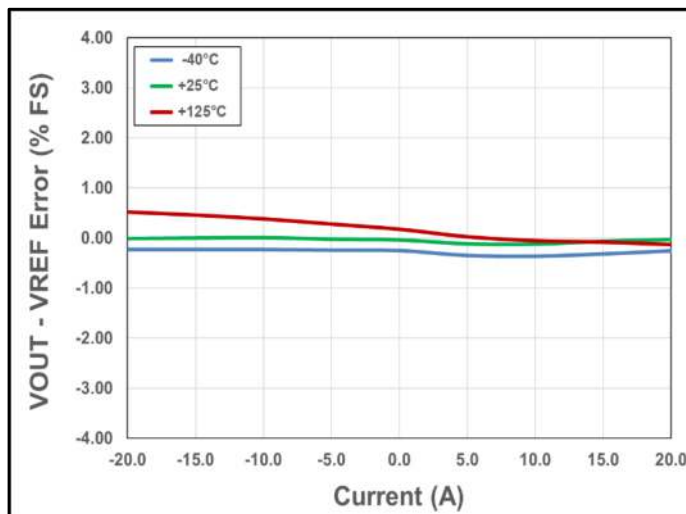


Figure 22. VOUT - VREF Error vs. Current vs. Temperature

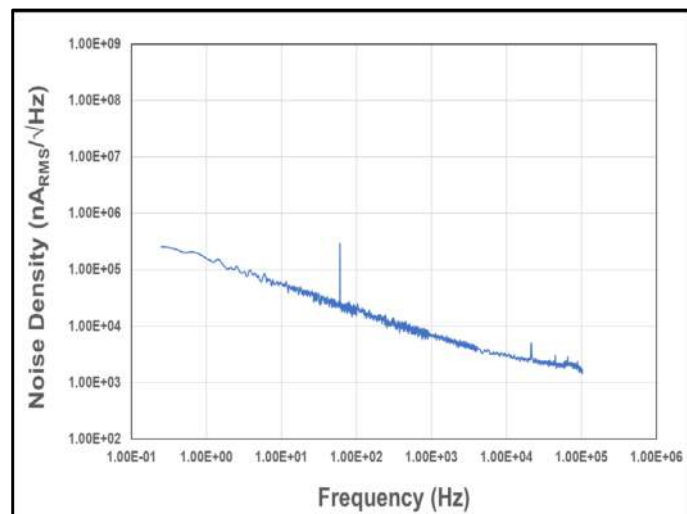


Figure 23. Noise Density vs. Frequency

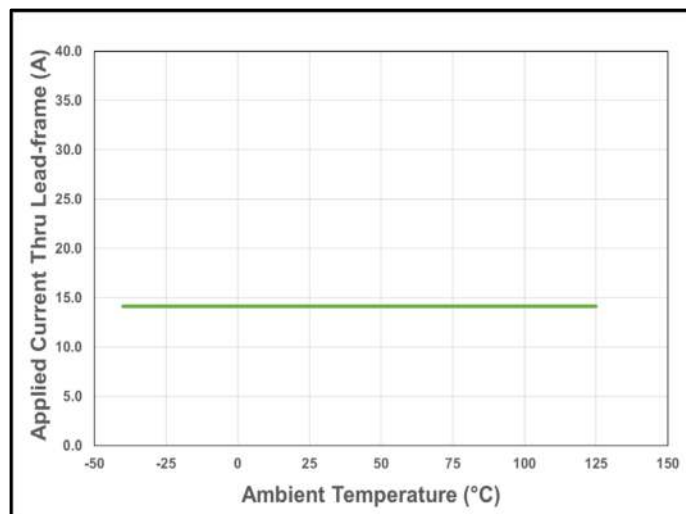


Figure 24. CT430 Current De-rating Curve for 20 A_{PK} (14.1 A_{DC})

CT430-xSWF30DR: 0 A to +30 A

Unless otherwise specified: $V_{CC} = 4.75\text{ V to }5.50\text{ V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$, $C_{BYP} = 1.0\text{ }\mu\text{F}$. Typical values are $V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{RANGE}	Current Range		0		+30	A
V _{OQ}	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	0.495	0.500	0.505	V
S	Sensitivity	I _{RANGE(MIN)} ≤ I _P ≤ I _{RANGE(MAX)}		133.3		mV/A
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB C _{FILTER} = 5 pF		1.0		MHz
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		10.0		mA _{RMS}
OUT Accuracy Performance						
E _{OUT}	Total Output Error	I _P = I _{P(MAX)}		±0.7	±1.0	% FS
E _{LIN}	Non-Linearity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.1		% FS
E _{SENS}	Sensitivity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.6		% FS
V _{OFFSET}	Offset Voltage ⁽¹⁾	I _P = 0 A, T _A = -40°C to +125°C		±13.5		mV
				±0.3		% FS
V _{OUT} – V _{REF} Accuracy Performance						
E _{OUT-VREF}	V _{OUT} – V _{REF} Error	I _P = I _{P(MAX)} , V _{CC} = 5.0 V T _A = -40°C to +125°C			±1.0	% FS
V _{OUT} - V _{REF}	OUT – V _{REF} Offset Voltage	V _{CC} = 5.0 V T _A = -40°C to +125°C		±5.0		mV
Lifetime Drift						
E _{TOT_DRIFT}	Total Output Error Lifetime Drift ⁽¹⁾	I _P = I _{P(MAX)}		±1.0		% FS

(1) Guaranteed by design and characterization; not tested in production.

Electrical Characteristics for CT430-xSWF30DR

$V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$ and $C_{BYP} = 1.0\text{ }\mu\text{F}$ (unless otherwise specified)

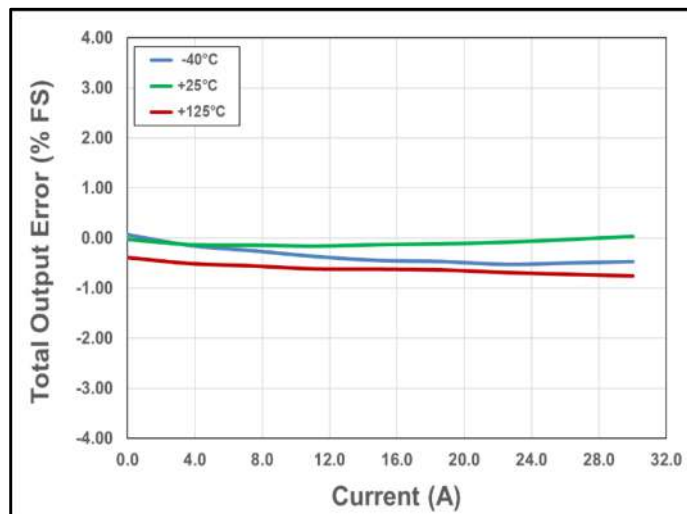


Figure 25. Total Output Error vs. Current vs. Temperature

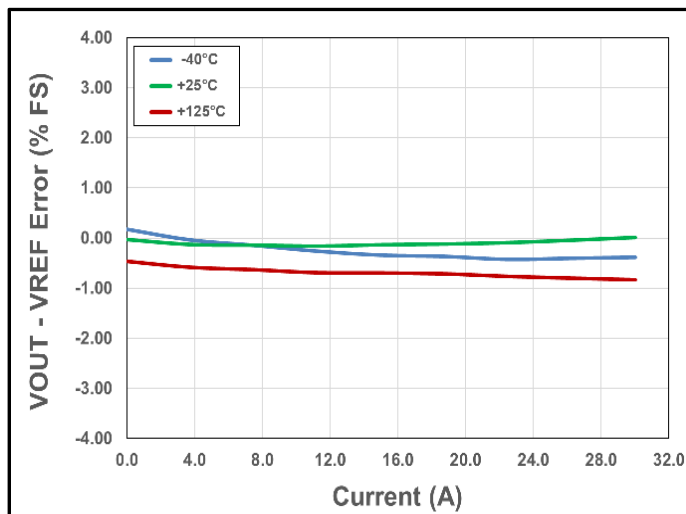


Figure 26. VOUT - VREF Error vs. Current vs. Temperature

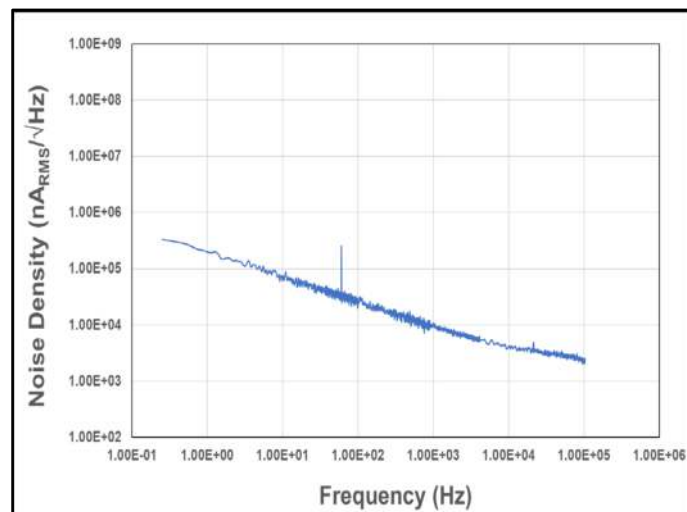


Figure 27. Noise Density vs. Frequency

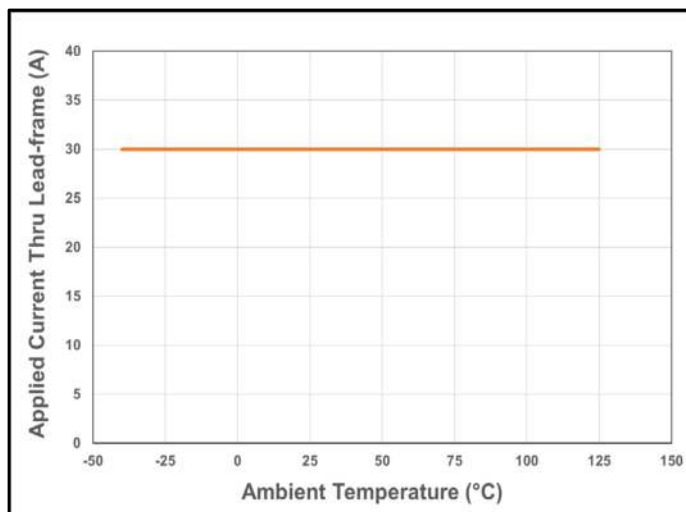


Figure 28. CT430 Current De-rating Curve for 30 A_{DC}

CT430-xSWF30MR: -30 A to +30 A

Unless otherwise specified: $V_{CC} = 4.75\text{ V to }5.50\text{ V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$, $C_{BYP} = 1.0\text{ }\mu\text{F}$. Typical values are $V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{RANGE}	Current Range		-30		+30	A
V _{OQ}	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	2.495	2.500	2.505	V
S	Sensitivity	I _{RANGE(MIN)} ≤ I _P ≤ I _{RANGE(MAX)}		66.7		mV/A
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB C _{FILTER} = 5 pF		1.0		MHz
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		11.5		mA _{RMS}
OUT Accuracy Performance						
E _{OUT}	Total Output Error	I _P = I _{P(MAX)}		±0.5	±1.0	% FS
E _{LIN}	Non-Linearity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.1		% FS
E _{SENS}	Sensitivity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.4		% FS
V _{OFFSET}	Offset Voltage ⁽¹⁾	I _P = 0 A, T _A = -40°C to +125°C		±9.0		mV
				±0.2		% FS
V _{OUT} – V _{REF} Accuracy Performance						
E _{OUT-VREF}	V _{OUT} – V _{REF} Error	I _P = I _{P(MAX)} , V _{CC} = 5.0 V T _A = -40°C to +125°C			±1.0	% FS
V _{OUT} - V _{REF}	OUT – V _{REF} Offset Voltage	V _{CC} = 5.0 V T _A = -40°C to +125°C		±5.0		mV
Lifetime Drift						
E _{TOT_DRIFT}	Total Output Error Lifetime Drift ⁽¹⁾	I _P = I _{P(MAX)}		±1.0		% FS

(1) Guaranteed by design and characterization; not tested in production.

Electrical Characteristics for CT430-xSWF30MR

$V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$ and $C_{BYP} = 1.0\text{ }\mu\text{F}$ (unless otherwise specified)

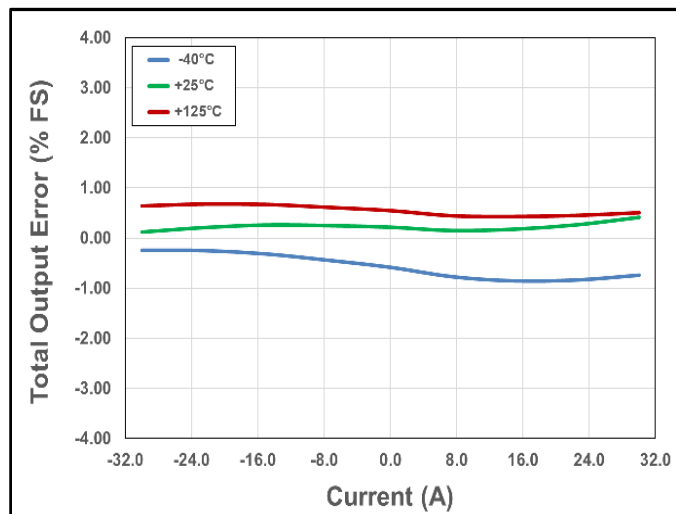


Figure 29. Total Output Error vs. Current vs. Temperature

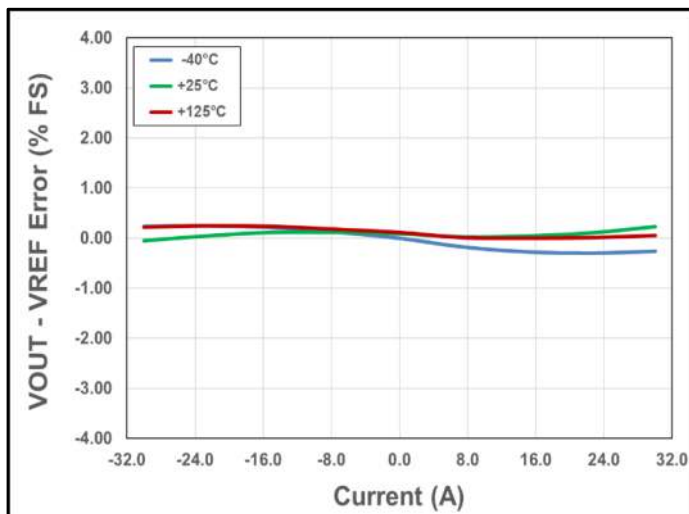


Figure 30. VOUT - VREF Error vs. Current vs. Temperature

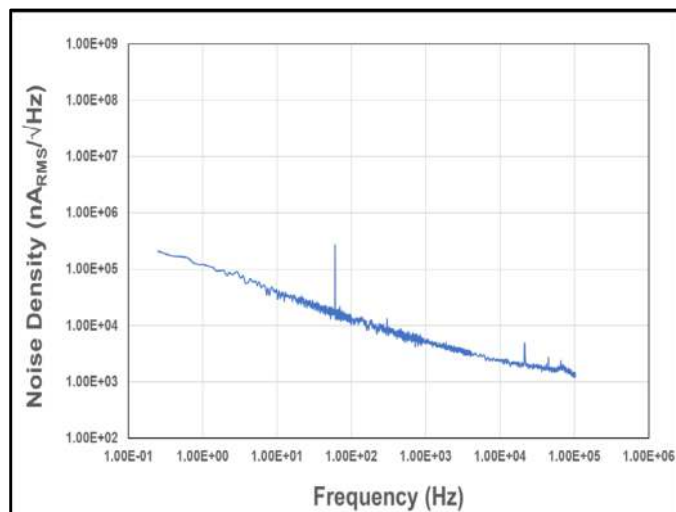


Figure 31. Noise Density vs. Frequency

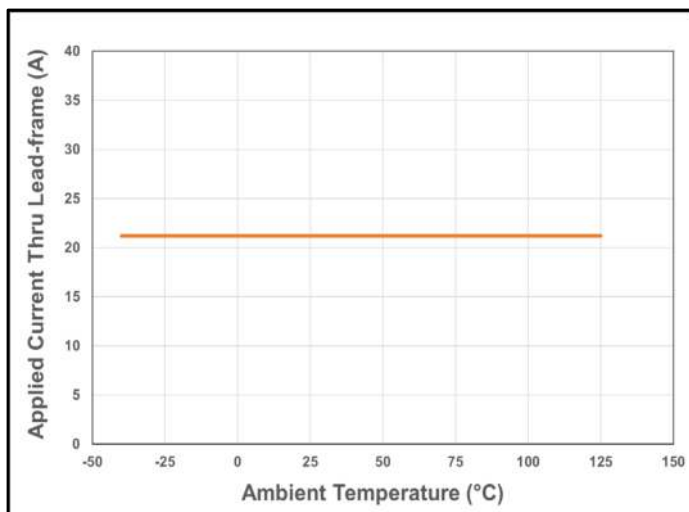


Figure 32. CT430 Current De-rating Curve for 30 A_{PK} (21.2 A_{DC})

CT430-xSWF50DR: 0 A to +50 A

Unless otherwise specified: $V_{CC} = 4.75\text{ V to }5.50\text{ V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$, $C_{BYP} = 1.0\text{ }\mu\text{F}$. Typical values are $V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{RANGE}	Current Range		0		+50	A
V _{OQ}	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	0.495	0.500	0.505	V
S	Sensitivity	I _{RANGE(MIN)} ≤ I _P ≤ I _{RANGE(MAX)}		80		mV/A
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB		1.0		MHz
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		10.0		mA _{RMS}
OUT Accuracy Performance						
E _{OUT}	Total Output Error	I _P = I _{P(MAX)}		±0.7	±1.5	% FS
E _{LIN}	Non-Linearity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.2		% FS
E _{SENS}	Sensitivity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.6		% FS
V _{OFFSET}	Offset Voltage ⁽¹⁾	I _P = 0 A, T _A = -40°C to +125°C		±12.9		mV
				±0.3		% FS
V _{OUT} – V _{REF} Accuracy Performance						
E _{OUT-VREF}	V _{OUT} – V _{REF} Error	I _P = I _{P(MAX)} , V _{CC} = 5.0 V T _A = -40°C to +125°C			±1.0	% FS
V _{OUT} - V _{REF}	OUT – V _{REF} Offset Voltage	V _{CC} = 5.0 V T _A = -40°C to +125°C		±5.0		mV
Lifetime Drift						
E _{TOT_DRIFT}	Total Output Error Lifetime Drift ⁽¹⁾	I _P = I _{P(MAX)}		±1.0		% FS

(1) Guaranteed by design and characterization; not tested in production.

Electrical Characteristics for CT430-xSWF50DR

$V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$ and $C_{BYP} = 1.0\text{ }\mu\text{F}$ (unless otherwise specified)

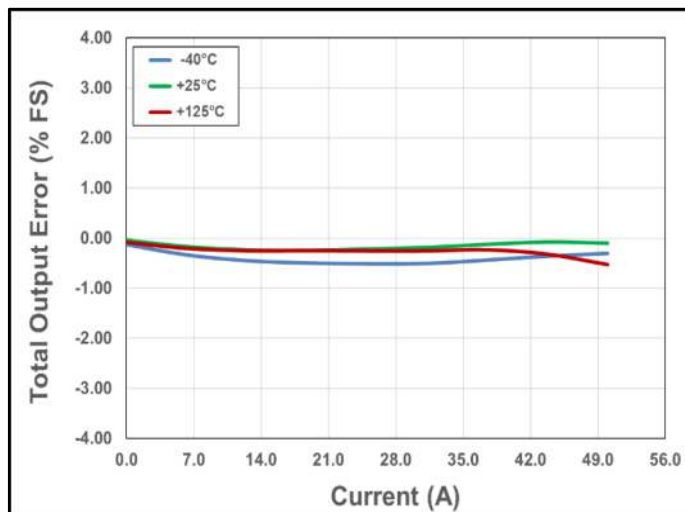


Figure 33. Total Output Error vs. Current vs. Temperature

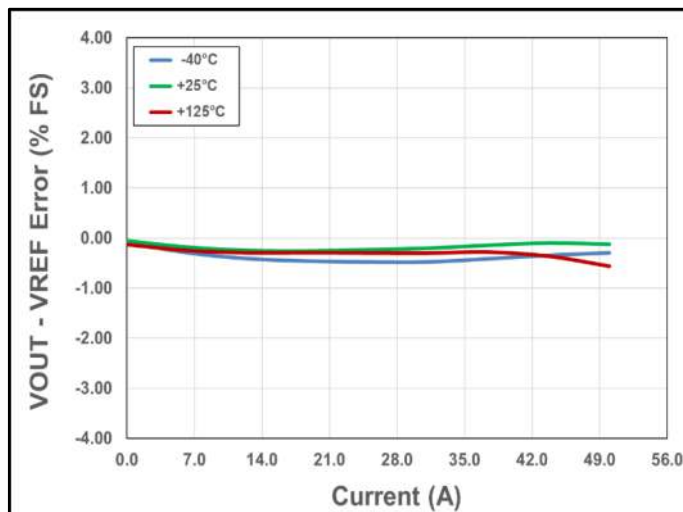


Figure 34. $V_{OUT} - V_{REF}$ Error vs. Current vs. Temperature

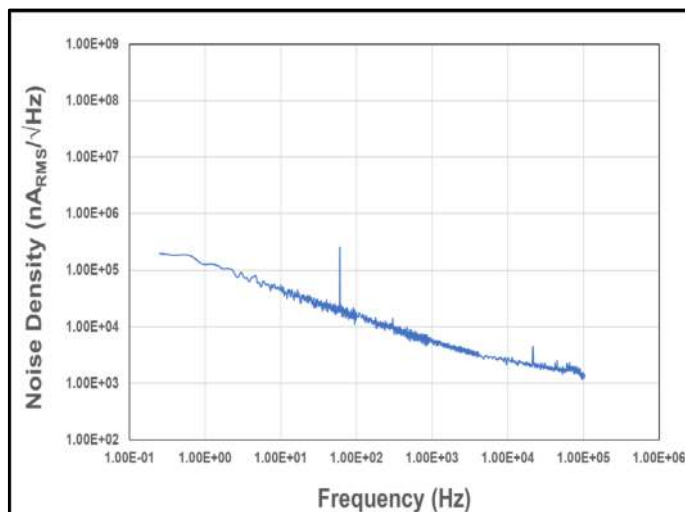


Figure 35. Noise Density vs. Frequency

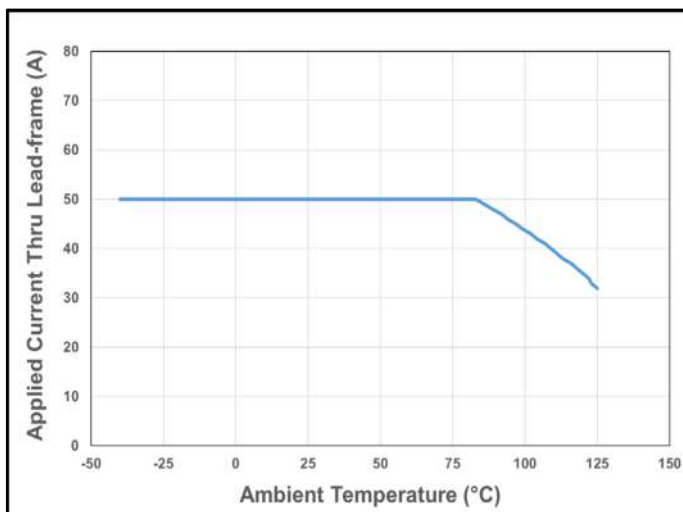


Figure 36. CT430 Current De-rating Curve for 50 A_{DC}

CT430-xSWF50MR: -50 A to +50 A

Unless otherwise specified: $V_{CC} = 4.75\text{ V to }5.50\text{ V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$, $C_{BYP} = 1.0\text{ }\mu\text{F}$. Typical values are $V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{RANGE}	Current Range		-50		+50	A
V _{OQ}	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	2.495	2.500	2.505	V
S	Sensitivity	I _{RANGE(MIN)} ≤ I _P ≤ I _{RANGE(MAX)}		40		mV/A
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB		1.0		MHz
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		14.0		mA _{RMS}
OUT Accuracy Performance						
E _{OUT}	Total Output Error	I _P = I _{P(MAX)}		±0.5	±1.0	% FS
E _{LIN}	Non-Linearity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.1		% FS
E _{SENS}	Sensitivity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.5		% FS
V _{OFFSET}	Offset Voltage ⁽¹⁾	I _P = 0 A, T _A = -40°C to +125°C		±10.9		mV
				±0.3		% FS
V _{OUT} – V _{REF} Accuracy Performance						
E _{OUT-VREF}	V _{OUT} – V _{REF} Error	I _P = I _{P(MAX)} , V _{CC} = 5.0 V T _A = -40°C to +125°C			±1.0	% FS
V _{OUT} - V _{REF}	OUT – V _{REF} Offset Voltage	V _{CC} = 5.0 V T _A = -40°C to +125°C		±5.0		mV
Lifetime Drift						
E _{TOT_DRIFT}	Total Output Error Lifetime Drift ⁽¹⁾	I _P = I _{P(MAX)}		±1.0		% FS

(1) Guaranteed by design and characterization; not tested in production.

Electrical Characteristics for CT430-xSWF50MR

$V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$ and $C_{BYP} = 1.0\text{ }\mu\text{F}$ (unless otherwise specified)

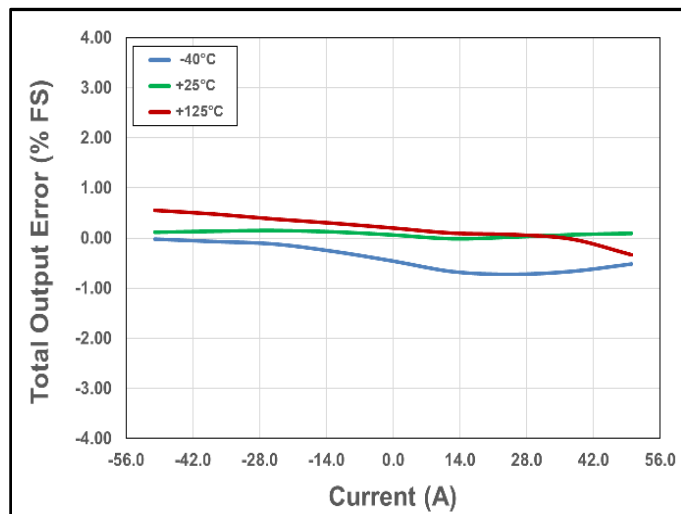


Figure 37. Total Output Error vs. Current vs. Temperature

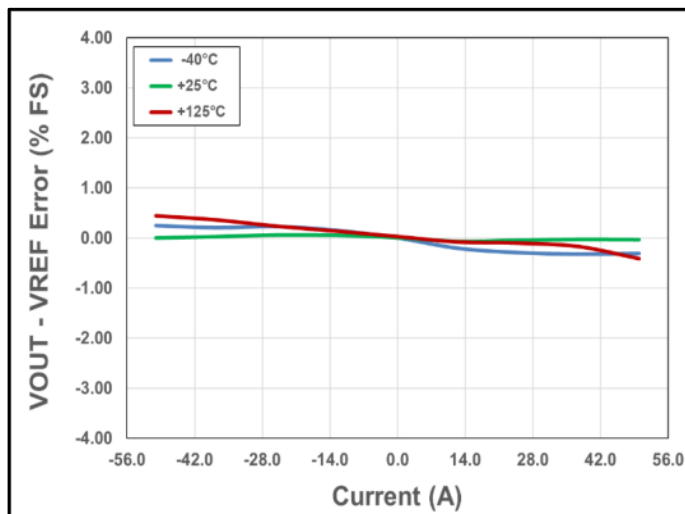


Figure 38. VOUT - VREF Error vs. Current vs. Temperature

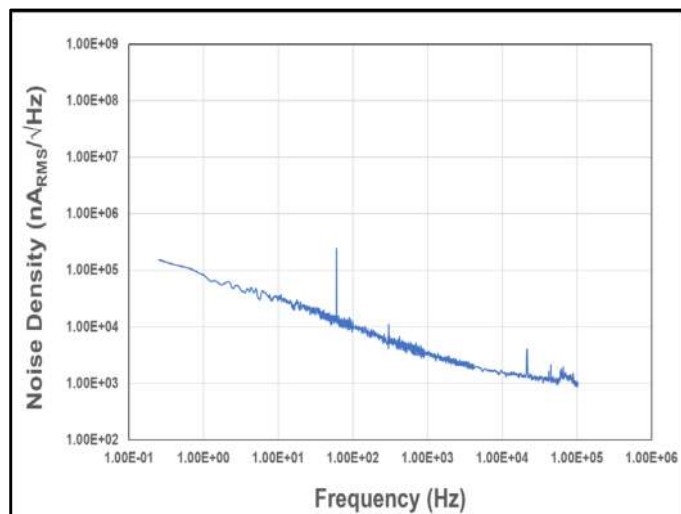


Figure 39. Noise Density vs. Frequency

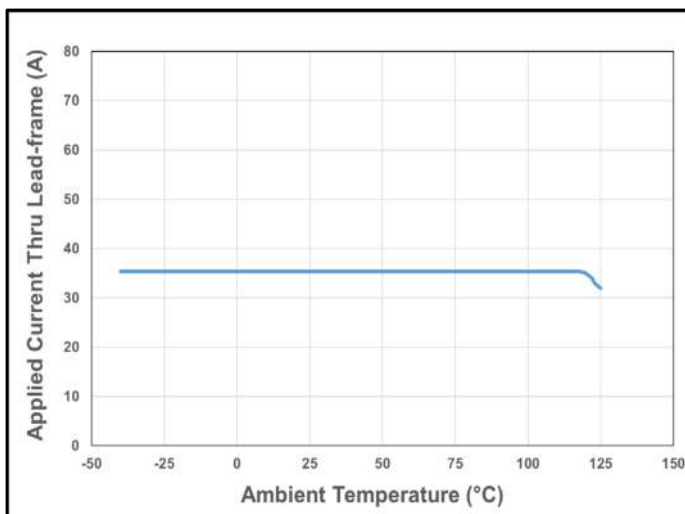


Figure 40. CT430 Current De-rating Curve for 50 A_{PK} (35.4 A_{DC})

CT430-xSWF65DR: 0 A to +65 A

Unless otherwise specified: $V_{CC} = 4.75\text{ V to }5.50\text{ V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$, $C_{BYP} = 1.0\text{ }\mu\text{F}$. Typical values are $V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{RANGE}	Current Range		0		+65	A
V _{OQ}	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	0.495	0.500	0.505	V
S	Sensitivity	I _{RANGE(MIN)} ≤ I _P ≤ I _{RANGE(MAX)}		61.5		mV/A
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB		1.0		MHz
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		10.0		mA _{RMS}
t _{IP(MAX)}	Maximum Time @ I _{P(MAX)} ⁽¹⁾					s
OUT Accuracy Performance						
E _{OUT}	Total Output Error	I _P = I _{P(MAX)}		±0.7	±1.5	% FS
E _{LIN}	Non-Linearity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.2		% FS
E _{SENS}	Sensitivity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.4		% FS
V _{OFFSET}	Offset Voltage ⁽¹⁾	I _P = 0 A, T _A = -40°C to +125°C		±3.0		mV
				±0.1		% FS
V _{OUT} – V _{REF} Accuracy Performance						
E _{OUT-VREF}	V _{OUT} – V _{REF} Error	I _P = I _{P(MAX)} , V _{CC} = 5.0 V T _A = -40°C to +125°C			±1.0	% FS
V _{OUT} - V _{REF}	OUT – V _{REF} Offset Voltage	V _{CC} = 5.0 V T _A = -40°C to +125°C		±5.0		mV
Lifetime Drift						
E _{TOT_DRIFT}	Total Output Error Lifetime Drift ⁽¹⁾	I _P = I _{P(MAX)}		±1.0		% FS

(2) Guaranteed by design and characterization; not tested in production.

Electrical Characteristics for CT430-xSWF65DR

$V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$ and $C_{BYP} = 1.0\text{ }\mu\text{F}$ (unless otherwise specified)

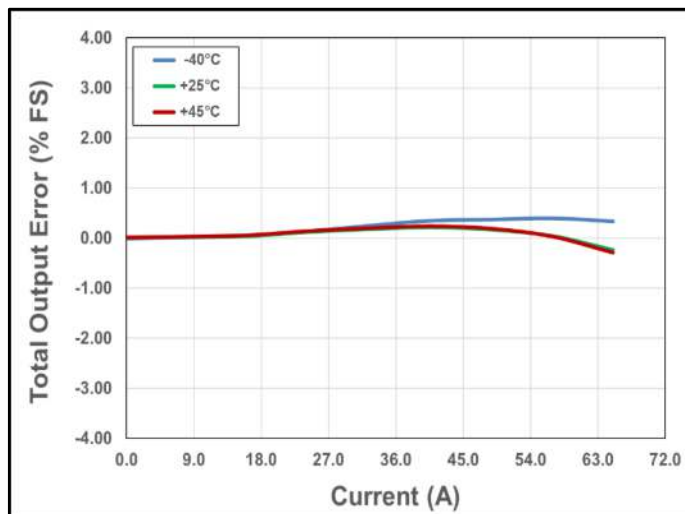


Figure 41. Total Output Error vs. Current vs. Temperature

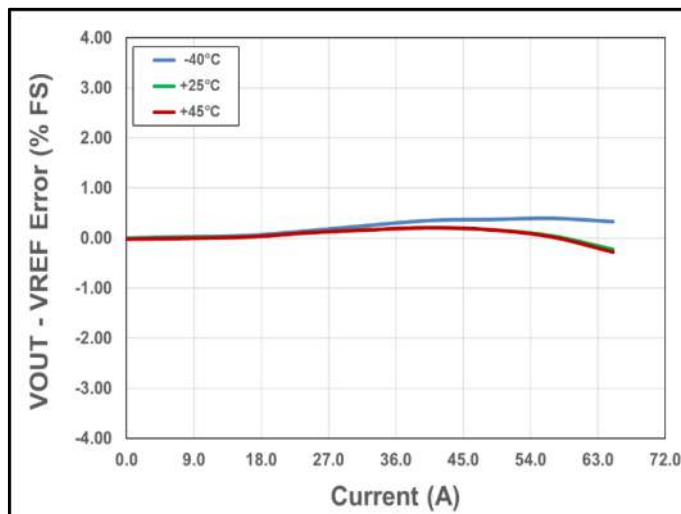


Figure 42. $V_{OUT} - V_{REF}$ Error vs. Current vs. Temperature

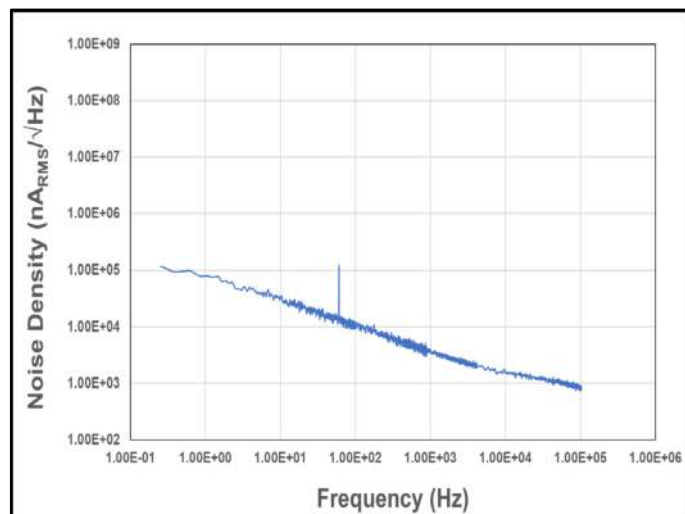


Figure 43. Noise Density vs. Frequency

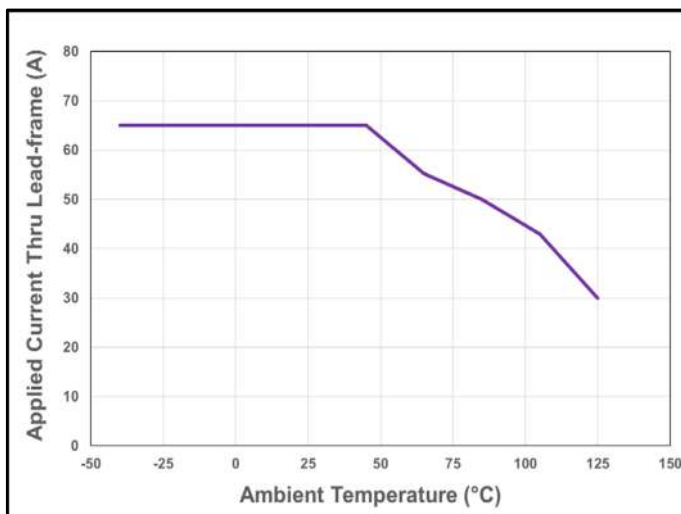


Figure 44. CT430 Current De-rating Curve for 65 A_{DC}

CT430-xSWF65MR: -65 A to +65 A

Unless otherwise specified: $V_{CC} = 4.75\text{ V to }5.50\text{ V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$, $C_{BYP} = 1.0\text{ }\mu\text{F}$. Typical values are $V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{RANGE}	Current Range		-65		+65	A
V _{OQ}	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	2.495	2.500	2.505	V
S	Sensitivity	I _{RANGE(MIN)} ≤ I _P ≤ I _{RANGE(MAX)}		30.8		mV/A
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB		1.0		MHz
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		13.5		mA _{RMS}
t _{IP(MAX)}	Maximum Time @ I _{P(MAX)} ⁽¹⁾					s
OUT Accuracy Performance						
E _{OUT}	Total Output Error	I _P = I _{P(MAX)}		±0.5	±1.0	% FS
E _{LIN}	Non-Linearity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.2		% FS
E _{SENS}	Sensitivity Error ⁽¹⁾	I _P = I _{P(MAX)} , T _A = -40°C to +125°C		±0.3		% FS
V _{OFFSET}	Offset Voltage ⁽¹⁾	I _P = 0 A, T _A = -40°C to +125°C		±3.0		mV
				±0.1		% FS
V _{OUT} – V _{REF} Accuracy Performance						
E _{OUT-VREF}	V _{OUT} – V _{REF} Error	I _P = I _{P(MAX)} , V _{CC} = 5.0 V T _A = -40°C to +125°C			±1.0	% FS
V _{OUT} - V _{REF}	OUT – V _{REF} Offset Voltage	V _{CC} = 5.0 V T _A = -40°C to +125°C		±5.0		mV
Lifetime Drift						
E _{TOT_DRIFT}	Total Output Error Lifetime Drift ⁽¹⁾	I _P = I _{P(MAX)}		±1.0		% FS

(2) Guaranteed by design and characterization; not tested in production.

Electrical Characteristics for CT430-xSWF65MR

$V_{CC} = 5.00\text{ V}$ and $T_A = +25^\circ\text{C}$ and $C_{BYP} = 1.0\text{ }\mu\text{F}$ (unless otherwise specified)

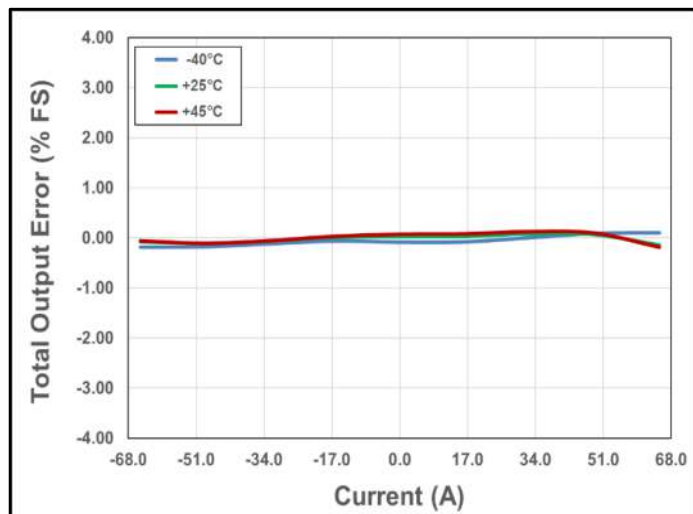


Figure 45. Total Output Error vs. Current vs. Temperature

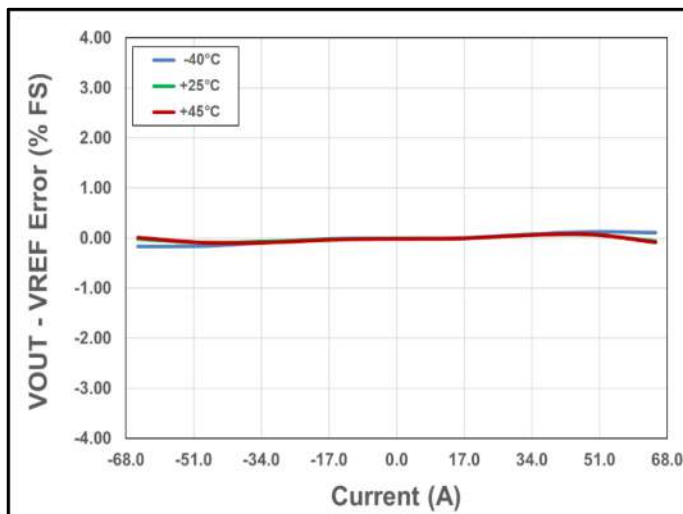


Figure 46. $V_{OUT} - V_{REF}$ Error vs. Current vs. Temperature

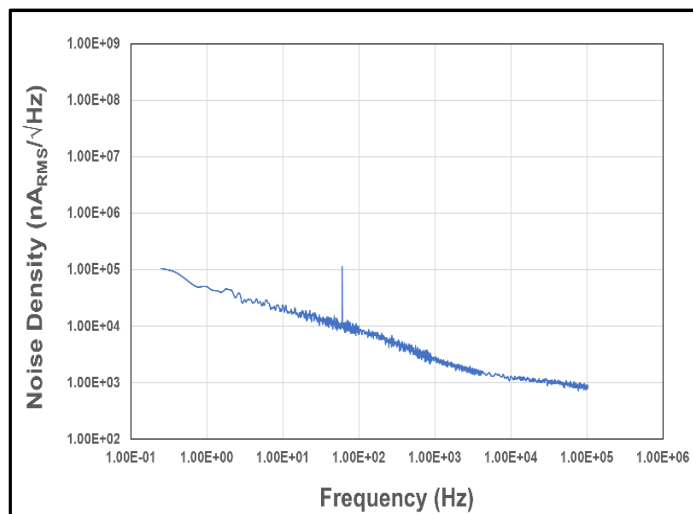


Figure 47. Noise Density vs. Frequency

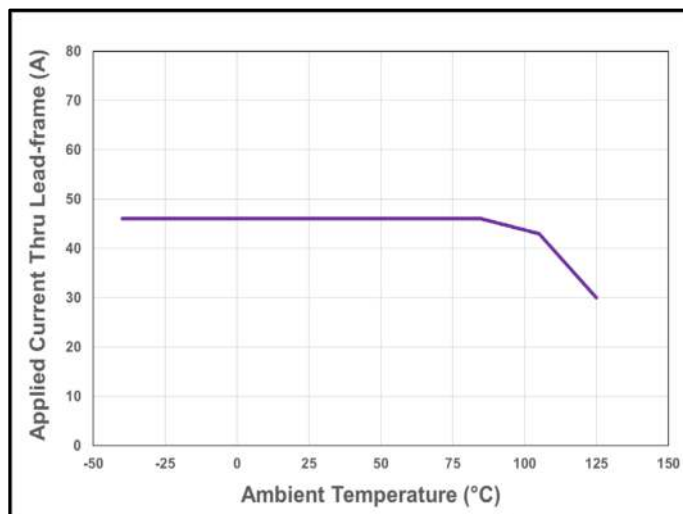


Figure 48. CT430 Current De-rating Curve for 65 A_{PK} (46.0 A_{DC})

Circuit Description

Overview

The CT430 is a very high accuracy contact current sensor with an integrated current carrying conductor (CCC) that handles up to 65 A. It has very high sensitivity and a wide dynamic range with excellent accuracy (very low total output error) across temperature. This current sensor supports eight (8) current ranges:

- 0 A to +20A
- -20 A to +20 A
- 0 A to +30 A
- -30 A to +30 A
- 0 A to +50 A
- -50 A to +50 A
- 0 A to +65 A
- -65 A to +65 A

When current is flowing through the CCC, the XtemeSense TMR sensors inside the chip senses the field which in turn generates differential voltage signals that then goes through the Analog Front-End (AFE) to output a current measurement with less than $\pm 1.0\%$ Full-Scale (FS) total output error (E_{OUT}).

The chip is designed to enable a very fast response time of 300 ns for the current measurement from the OUT pin as the bandwidth for the CT430 is 1.0 MHz. Even with a high bandwidth, the chip consumes a minimal amount of power.

Linear Output Current Measurement

The CT430 provides a continuous linear analog output voltage which represents the current measurement. The output voltage range of OUT is from 0.50 V to 4.50 V with a V_{OQ} of 0.50 V and 2.50 V for unidirectional and bidirectional currents, respectively. Figure 49 illustrates the output voltage range of the OUT pin as a function of the measured current.

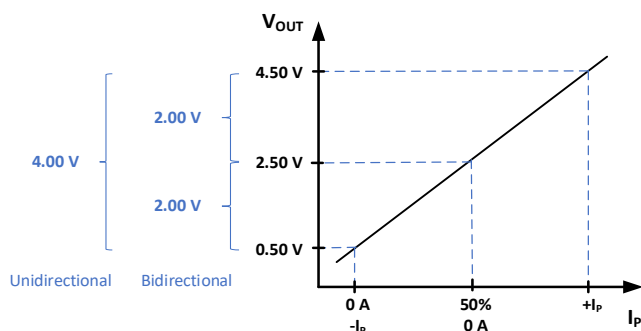


Figure 49. Linear Output Voltage Range (OUT) vs. Measured Current (I_P)

Filter Function (FILTER)

The CT430 has a pin for the FILTER function which will enable it to improve the noise performance by changing the cut-off frequency. The bandwidth of the CT430 is 1.0 MHz however by adding a capacitor to the FILTER pin which will be in series with an internal resistance of approximately 15 k Ω will set the cut-off frequency to reduce the noise. .

Table 2 shows the capacitor values required to achieve four (4) cut-off frequencies.

Table 2. R-C Filter Options for FILTER Pin

Cut-off Frequency	C_{FILTER} (pF)	Capacitor Part Number
100 kHz	91	GRM0225C1C910JA02
250 kHz	33	GRM0225C1C330JA02
500 kHz	16	GRM0225C1C160JA03
1.0 MHz	5	GRM0225C1C5R0CA03

If the FILTER pin is not used, then it should be left unconnected (No Connect).

Voltage Reference Function (VREF)

The CT430 has a reference voltage (VREF) pin that may be used as an output voltage reference for AC or DC current measurements. The VREF pin should be connected to a buffer circuit.

If the VREF is not used, then it should be left unconnected.

Sensitivity

The Sensitivity (S) is a change in CT430's output in response to a change in 1 A of current flowing through the CCC. It is defined by the product of the magnetic circuit sensitivity (G/A, where 1.0 G = 0.1 mT) and the chip's linear amplifier gain (mV/G). Therefore, the result of this gives a sensitivity unit of mV/A. The CT430 is factory calibrated to optimize the sensitivity for the full scale of the device's dynamic range.

Total Output Error

The Total Output Error is the difference between the current measured by CT430 and the actual current, relative to the actual current. It is equivalent to the ratio between the difference of the ideal and actual voltage to the ideal sensitivity multiplied by the current flowing through the primary conductor (CCC). The following

equation defines the Total Output Error (E_{OUT}) for the CT430:

$$E_{OUT} = \frac{V_{IOUT_IDEAL}(I_P) - V_{IOUT}(I_P)}{S_{IDEAL}(I_P) \times I_P}$$

The E_{OUT} incorporates all sources of error and is a function of the sensed current (I_P) from CT430. At high current levels, the E_{OUT} will be dominated by the sensitivity error whereas at low current, the dominant characteristic is the offset voltage. Figure 50 shows the behavior of E_{OUT} versus I_P . When I_P goes to 0 from both directions, the curves exhibit asymptotic behavior i.e., E_{OUT} approaches infinity.

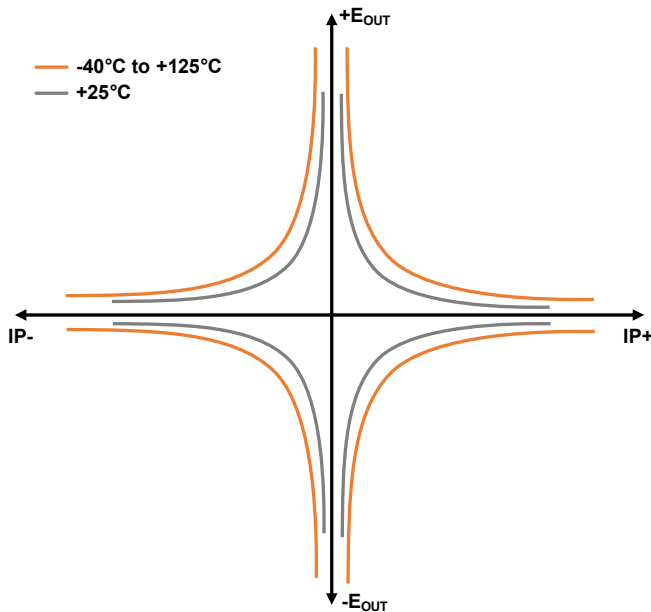


Figure 50. Total Output Error (E_{OUT}) vs. Sensed Current (I_P)

The CT430 achieves a total output error (E_{OUT}) that is less than $\pm 1.0\%$ of Full-Scale (FS) over supply voltage and temperature. It is designed with innovative and proprietary TMR sensors and circuit blocks to provide very accurate current measurements regardless of the operating conditions.

Sensitivity Error

The sensitivity error (E_{SENS}) is the sensitivity temperature drift error for unipolar or DC current. It is calculated using the equation below:

$$E_{SENS} = \left(\frac{S_{MEASURED}}{S} - 1 \right) \times 100\%$$

For bipolar or AC current, the E_{SENS} is calculated by dividing the equation by 2.

Power-On Time (t_{ON})

The Power-On Time (t_{ON}) of 100 μs is the amount of time required by CT430 to start up, fully power the chip and becoming fully operational from the moment the supply voltage is greater than the UVLO voltage. This time includes the ramp up time and the settling time (within 10% of steady-state voltage) after the power supply has reached the minimum V_{CC} .

Response Time ($t_{RESPONSE}$)

The Response Time ($t_{RESPONSE}$) of 300 ns for the CT430 is the time interval between the following terms:

1. When the primary current signal reaches 90% of its final value,
2. When the chip reaches 90% of its output corresponding to the applied current.

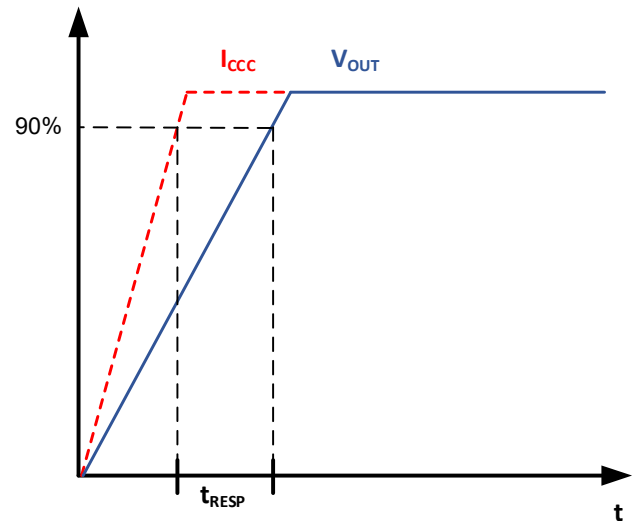


Figure 51. CT430 Response Time Curve

Rise Time (t_{RISE})

The CT430's rise time, t_{RISE} , is the time interval of when it reaches 10% and 90% of the full-scale output voltage. The t_{RISE} of the CT430 is 200 ns.

Propagation Delay (t_{DELAY})

The Propagation Delay (t_{DELAY}) is the time difference between these two events:

1. When the primary current reaches 20% of its final value
2. When the chip reaches 20% of its output corresponding to the applied current.

The CT430 has a propagation delay of 250 ns.

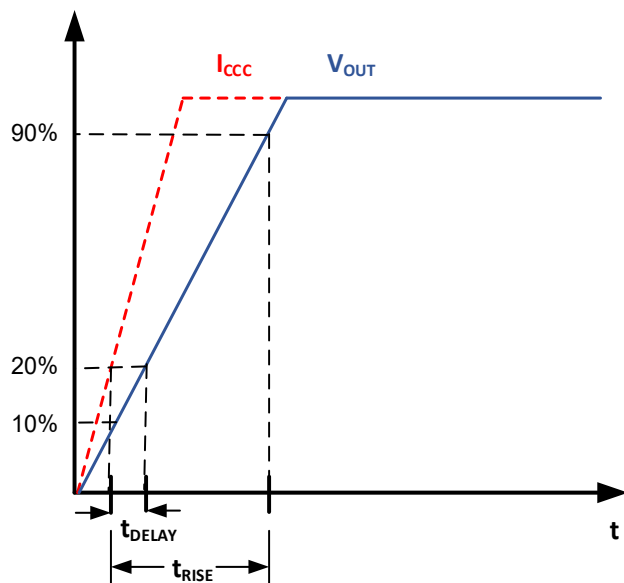


Figure 52. CT430 Propagation Delay and Rise Time Curve

Over-Current Detection (OCD)

The Over-Current Detection (OCD) circuitry detects measured current values that are 110% above the maximum current range value of the CT430 for the unipolar (DC current) variant. For the bipolar (AC current) variant of the CT430 it is greater than $\pm 110\%$ of the maximum current range. This will generate a fault signal via the Fault# Interrupt ($\overline{\text{FLT}}$) pin (LOW) to the host system's microcontroller. Once the measured current falls to 90% of the maximum current range for the DC current variant or $\pm 90\%$ for the AC current version then the fault will be cleared, and the $\overline{\text{FLT}}$ pin will go HIGH.

Under-Voltage Lockout (UVLO)

The Under-Voltage Lock-out protection circuitry of the CT430 is activated when the supply voltage (V_{CC}) falls below 2.45 V. The CT430 remains in a low quiescent state until V_{CC} rises above the UVLO threshold (2.50 V). In this condition where the V_{CC} is less than 2.45 V and UVLO is triggered, the output from the CT430 is not valid and the $\overline{\text{FLT}}$ pin will go LOW. Once the V_{CC} rises above 2.50 V then the UVLO is cleared, and the $\overline{\text{FLT}}$ pin will be HIGH.

Fault# Interrupt ($\overline{\text{FLT}}$)

The CT430 generates an active LOW digital fault signal via the $\overline{\text{FLT}}$ pin to interrupt the microcontroller to indicate a fault event has been triggered. It is an open drain output and requires a pull-up resistor with a value of 100 k Ω tied

to V_{CC} and a 1.0 nF capacitor is connected to ground. A fault signal will interrupt the host system for these events:

- OCD
- UVLO

The $\overline{\text{FLT}}$ signal will be asserted LOW whenever one of the above fault events occur. In the case of an UVLO event, the $\overline{\text{FLT}}$ pin will stay LOW until the fault is cleared and then go HIGH.

If the $\overline{\text{FLT}}$ is not used, then a 1.0 nF capacitor must be connected from the pin to ground.

Immunity to Common Mode Fields

The CT430 is housed in custom plastic package that utilizes a "U-shaped" lead-frame to reduce the common mode fields generated by external stray magnetic fields. With the "U-shaped" lead-frame, the stray fields cancel one another thus reducing electro-magnetic interference (EMI). The CT430 is able to achieve -54 dB of Common Mode Rejection Ratio (CMFRR).

Also, good PCB layout of the CT430 will optimize performance and reduce EMI. Please see the Applications Information section in this data sheet for recommendations on PCB layout.

Creepage and Clearance

Two important terms as it relates to isolation provided by the package are: creepage and clearance. Creepage is defined as the shortest distance across the surface of the package from one side the leads to the other side of the leads. The definition for clearance is the shortest distance between the leads of opposite side through the air. Figure 53 illustrates the creepage and clearance for the SOICW-16 package of the CT430.

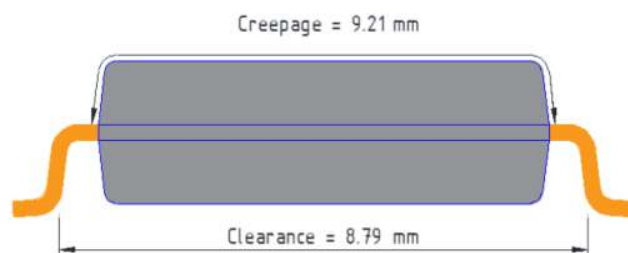


Figure 53. The Creepage and Clearance for the CT430's SOICW-16 package

Application

It is designed to support an operating voltage range of 4.75 V to 5.50 V, but it is ideal to use a 5.0 V power supply where the output tolerance is less than $\pm 5\%$.

A single 1.0 μF capacitor is needed for the VCC pin to reduce the noise from the power supply and other circuits. This capacitor should be placed as close as possible to the CT430 to minimize inductance and resistance between the two devices.

A capacitor may be added to the FILTER pin of the CT430 if there is a requirement to improve the noise

If the FILTER pin is not used, then it should not be connected (No Connect).

For the CT430, the FLT# pin is an open drain output. It requires a pull-up resistor value of 100 k Ω to be connected from the pin to V_{CC} and also a 1.0 nF capacitor to be connected from the pin to ground.

If the VREF pin is not needed in the application, then this pin should not be connected and be left floating.

Recommended PCB Layout

Since the CT430 can measure up to 65 A of current, special care must be taken in the printed circuit board (PCB) layout of the CT430 and the surrounding circuitry. It is recommended that the CCC pins be connected to as

much copper area as possible. For up to 30 A of current, 2 oz (or heavier) of copper can be used for the PCB traces. It is also recommended that 4 oz. or heavier copper be used for PCB traces when the CT430 is used to measure 50 A and 65 A of current. Additional layers of the PCB should also be used to carry current and be connected using the arrangement of vias.

Figure 55 and Figure 56 show the recommended the PCB layout for the 20 A, 30 A, 50 A and 65 A variants of the CT430. Please note that the traces connected to the IP+ and IP- pins of the CT430 are very wide with multiple vias such that it can handle the high current.

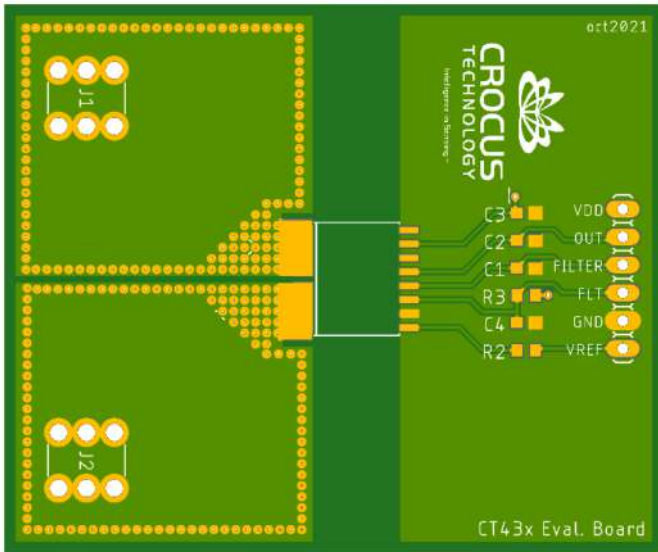


Figure 55. Recommended PCB Layout (Top Layer) for the 20 A to 65 A variants of the CT430.

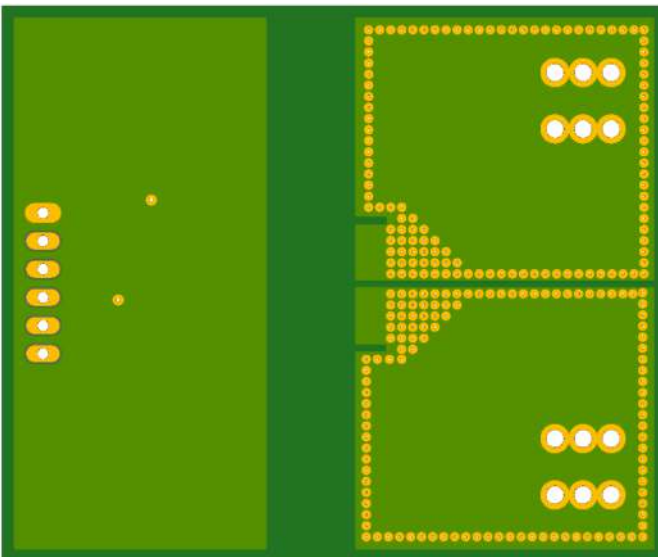


Figure 56. Recommended PCB Layout (Bottom Layer) for the 20 A to 65 A variants of the CT430.

SOICW-16 Package Drawing and Dimensions

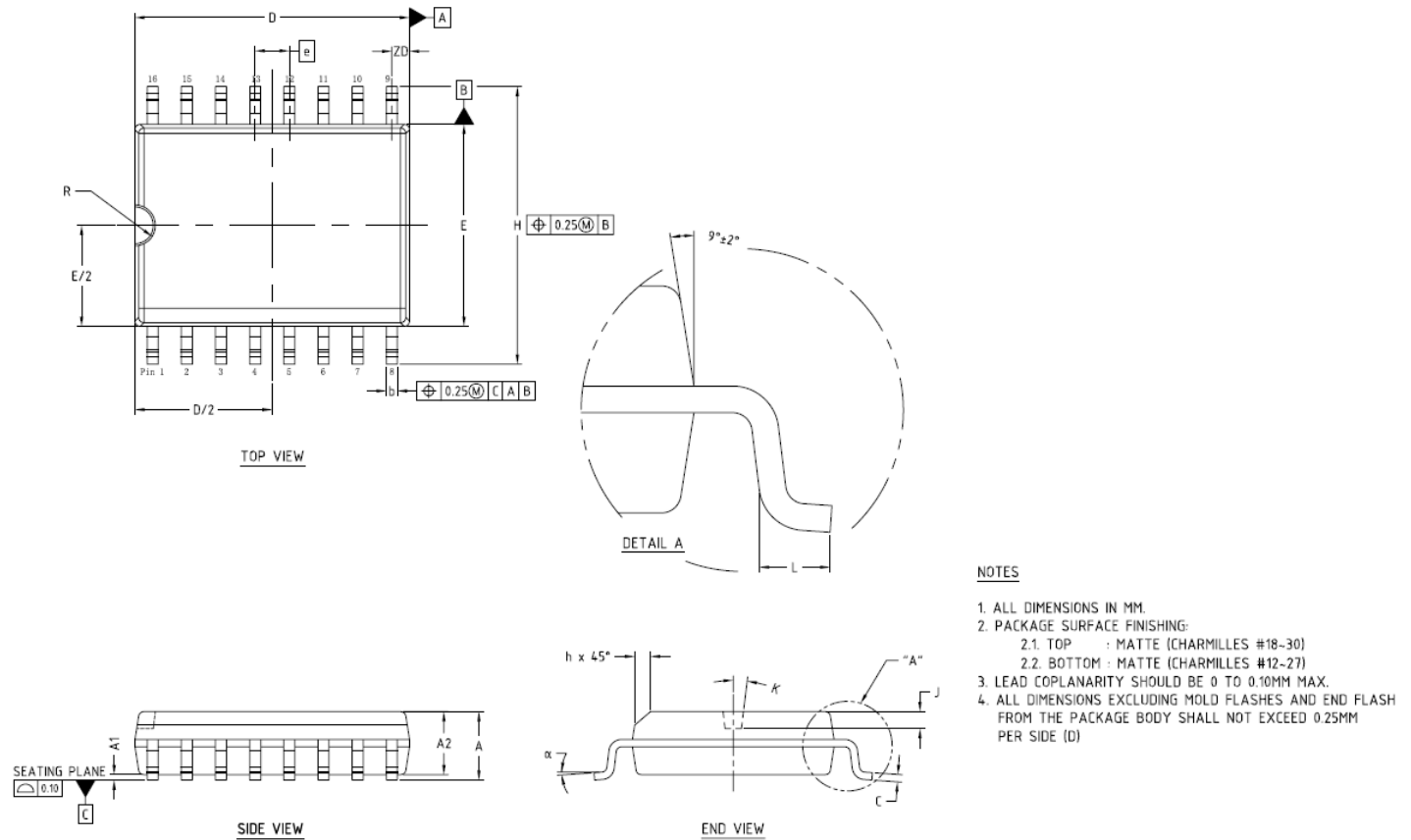


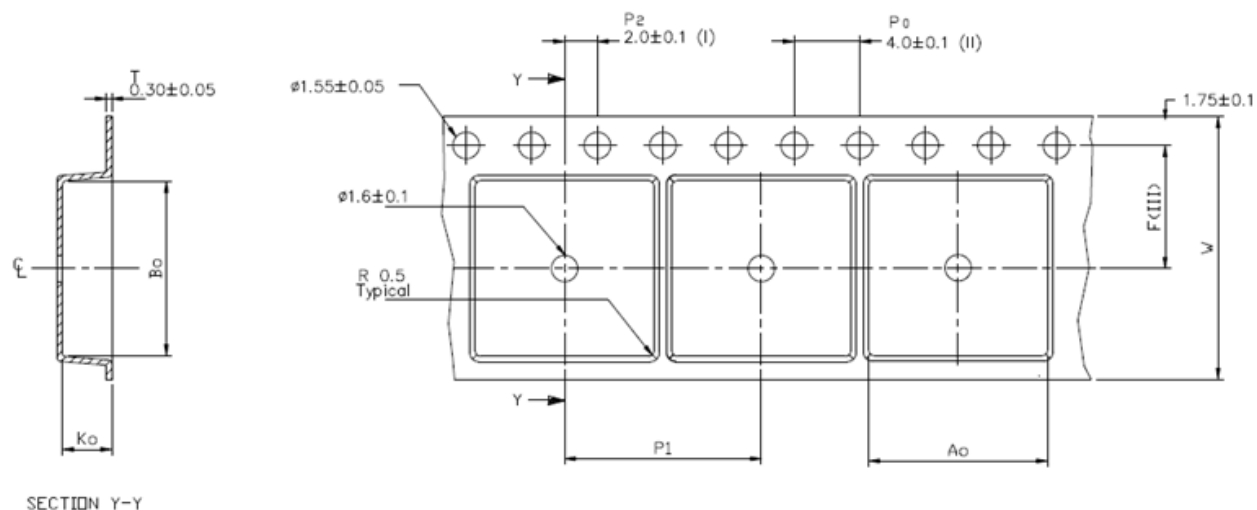
Figure 57. SOICW-16 Package Drawing

Table 3. CT430 SOICW-16 Package Dimensions

Symbol	Dimensions in Millimeters (mm)		
	Min.	Typ.	Max.
A	2.44	2.54	2.64
A1	0.10	0.20	0.30
A2	2.24	2.34	2.44
b	0.36	0.41	0.46
C	0.24	0.25	0.26
D	10.11	10.21	10.31
E	7.40	7.50	7.60
e	1.27 BSC		
H	10.11	10.31	10.51
h	0.31	0.51	0.71
J	0.53	0.63	0.73
K	7° BSC		
L	0.51	0.76	1.01
R	0.63	0.76	0.89
ZD	0.66 REF		
α	0°	-	8°

Crocus Technology provides package drawings as a service to customers considering or planning to use Crocus products in their designs. Drawings may change without notice. Please note the revision and date of the data sheet and contact a Crocus Technology representative to verify or obtain the most recent version. The package specifications do not expand the terms of Crocus Technology's worldwide terms and conditions, specifically the warranty therein, which covers Crocus Technology's products.

SOICW-16 Tape & Pocket Drawing and Dimensions



A_o	10.90 ± 0.1
B_o	10.70 ± 0.1
K_o	3.00 ± 0.1
F	7.50 ± 0.1
P_1	12.00 ± 0.1
W	16.00 ± 0.3

- (I) Measured from centreline of sprocket hole to centreline of pocket.
 (II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
 (III) Measured from centreline of sprocket hole to centreline of pocket.
 (IV) Other material available.
 (V) Typical SR of form tape Max 10^8 OHM/SQ

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 58. SOICW-16 Package Drawing

CT430 Tape Pocket Orientation

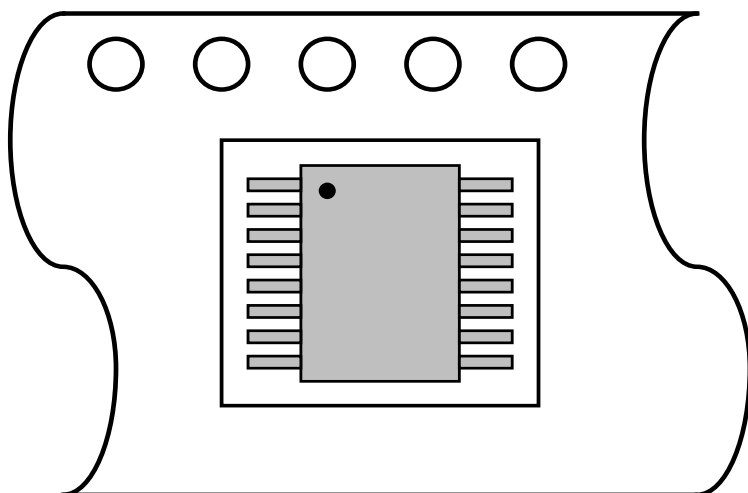


Figure 59. SOICW-16 Orientation in Tape Pocket

Package Information

Table 4. CT430 Package Information

Part Number	Package Type	# of Leads	Quantity per Reel	Lead Finish	MSL Rating ⁽²⁾	Operating Temperature ⁽³⁾	Device Marking ⁽⁴⁾
CT430-ESWF20DR	SOIC-W	16	1,000	Sn	3	-40°C to +85°C	CT430 SWF20DR YYWWLL
CT430-HSWF20DR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430 SWF20DR YYWWLL
CT430-ASWF20DR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430A SWF20DR YYWWLL
CT430-ESWF20MR	SOIC-W	16	1,000	Sn	3	-40°C to +85°C	CT430 SWF20MR YYWWLL
CT430-HSWF20MR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430 SWF20MR YYWWLL
CT430-ASWF20MR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430A SWF20MR YYWWLL
CT430-ESWF30DR	SOIC-W	16	1,000	Sn	3	-40°C to +85°C	CT430 SWF30DR YYWWLL
CT430-HSWF30DR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430 SWF30DR YYWWLL
CT430-ASWF30DR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430A SWF30DR YYWWLL
CT430-ESWF30MR	SOIC-W	16	1,000	Sn	3	-40°C to +85°C	CT430 SWF30MR YYWWLL
CT430-HSWF30MR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430 SWF30MR YYWWLL
CT430-ASWF30MR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430A SWF30MR YYWWLL
CT430-ESWF50DR	SOIC-W	16	1,000	Sn	3	-40°C to +85°C	CT430 SWF50DR YYWWLL

Part Number	Package Type	# of Leads	Quantity per Reel	Lead Finish	MSL Rating ⁽²⁾	Operating Temperature ⁽³⁾	Device Marking ⁽⁴⁾
CT430-HSWF50DR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430 SWF50DR YYWWLL
CT430-ASWF50DR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430A SWF50DR YYWWLL
CT430-ESWF50MR	SOIC-W	16	1,000	Sn	3	-40°C to +85°C	CT430 SWF50MR YYWWLL
CT430-HSWF50MR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430 SWF50MR YYWWLL
CT430-ASWF50MR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430A SWF50MR YYWWLL
CT430-ESWF65DR	SOIC-W	16	1,000	Sn	3	-40°C to +85°C	CT430 SWF65DR YYWWLL
CT430-HSWF65DR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430 SWF65DR YYWWLL
CT430-ASWF65DR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430A SWF65DR YYWWLL
CT430-ESWF65MR	SOIC-W	16	1,000	Sn	3	-40°C to +85°C	CT430 SWF65MR YYWWLL
CT430-HSWF65MR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430 SWF65MR YYWWLL
CT430-ASWF65MR	SOIC-W	16	1,000	Sn	3	-40°C to +125°C	CT430A SWF65MR YYWWLL

- (1) RoHS is defined as semiconductor products that are compliant to the current EU RoHS requirements. It also will meet the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Green is defined as the content of Chlorine (Cl), Bromine (Br) and Antimony Trioxide based flame retardants satisfy JS709B low halogen requirements of $\leq 1,000$ ppm.
- (2) MSL Rating = Moisture Sensitivity Level Rating as defined by JEDEC standard classifications.
- (3) Package will withstand ambient temperature range of -40°C to +125°C and storage temperature range of -65°C to +150°C.
- (4) Device Marking for CT430 is defined as CT430 SWFxxZR YYWWLL where the first 2 lines = part number, YY = year, WW = work week and LL = lot code.

Device Marking

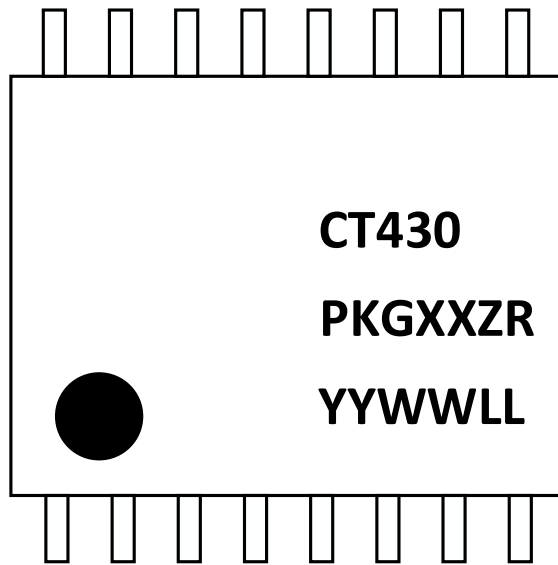
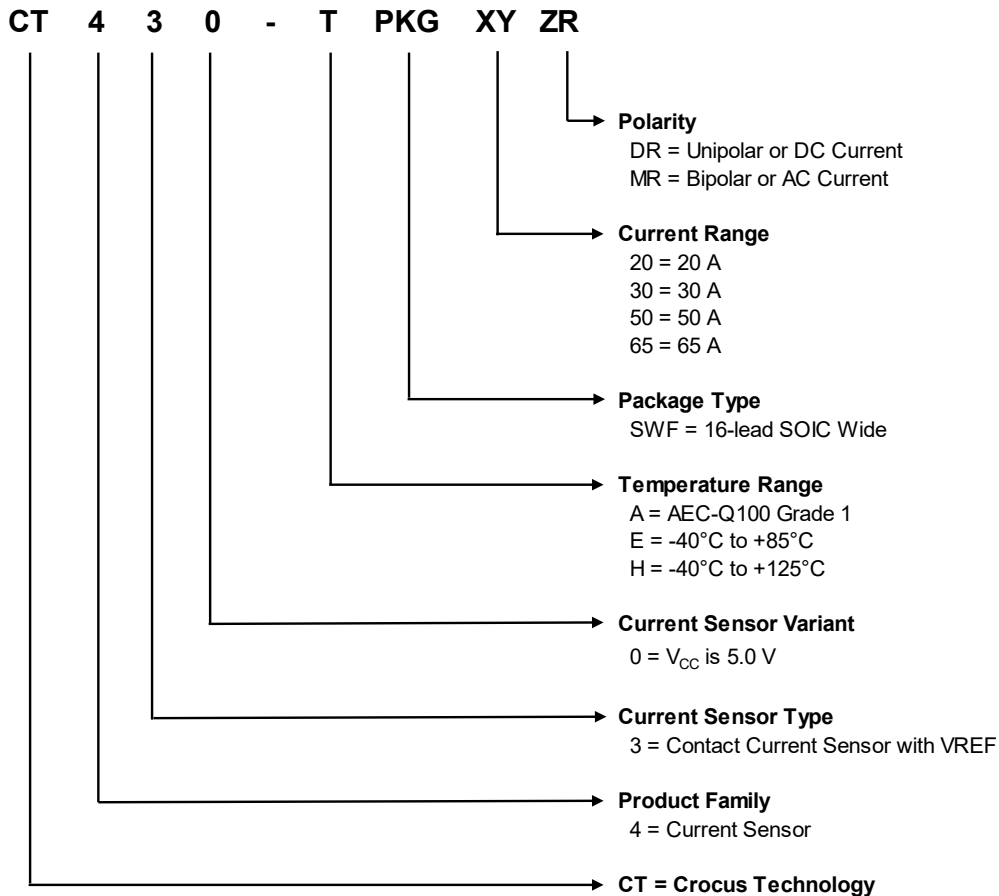


Figure 60. CT430 Device Marking for 16-lead Package

Row No.	Code	Definition
3	•	Pin 1 Indicator
1	CT430	Crocus Part Number
2	PKG	Package Type
2	XX	Maximum Current Rating
2	ZR	Current Range
3	YY	Calendar Year
3	WW	Work Week
3	LL	Lot Code

Table 5. CT430 Device Marking Definition for 16-lead SOIC-W Package

Part Number Ordering Legend



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